AFRL-AFOSR-VA-TR-2015-0250

N-FACE GAN ELECTRONICS FOR HETEROEPITAXIAL AND BONDED STRUCTURES

Umesh Mishra
UNIVERSITY OF CALIFORNIA SANTA BARBARA

08/27/2015
Final Report

Air Force Research Laboratory
AF Office Of Scientific Research (AFOSR)/ RTD
Arlington, Virginia 22203
Air Force Materiel Command

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	**2. REPORT TYPE**	**3. DATES COVERED** *(From - To)*
27-08-2015	Final Performance	01-04-2010 to 31-03-2015

4. TITLE AND SUBTITLE
N-FACE GAN ELECTRONICS FOR HETEROEPITAXIAL AND BONDED STRUCTURES

5a. CONTRACT NUMBER

5b. GRANT NUMBER
FA9550-10-1-0069

5c. PROGRAM ELEMENT NUMBER
61102F

6. AUTHOR(S)
Umesh Mishra

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
UNIVERSITY OF CALIFORNIA SANTA BARBARA
3227 CHEADLE HL
SANTA BARBARA, CA 93106-2050 US

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AF Office of Scientific Research
875 N. Randolph St. Room 3112
Arlington, VA 22203

10. SPONSOR/MONITOR'S ACRONYM(S)
AFRL/AFOSR RTD

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
A DISTRIBUTION UNLIMITED: PB Public Release

13. SUPPLEMENTARY NOTES

14. ABSTRACT
Wafer-bonded current aperture vertical transistors, BAVETs can obtain high frequency switching and breakdown. Transistor functionality has been obtained for such devices, but challenges such as high saturation voltages, on-resistance and low channel breakdown have limited performance. These performance anomalies may arise from the trap behavior of the waferbonded
interface (WBI). When passivating traps at the WBI, anomalies in a BAVET were eliminated. Its saturation voltage and drain resistance were lowered and critical field to impact-ionization was made higher through the optimization of the Npolar InGaN interlayer thickness and the utilization of the p-type III-As gate heterobarrier.

15. SUBJECT TERMS
BONDED, STRUCTURES

16. SECURITY CLASSIFICATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON**
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**			Umesh Mishra
Unclassified	Unclassified	Unclassified	UU		**19b. TELEPHONE NUMBER** *(Include area code)* 805-893-3586

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18

Final Performance Report

On

N-Face GaN Electronics for Heteroepitaxial and Bonded Structures

By

Professor Umesh K. Mishra

Electrical & Computer Engineering

Engineering Science Building (ESB) Rm 2215C

University of California, Santa Barbara

Santa Barbara, California 93106

Tel: (805) 893-3586

Fax: (805) 893-8714

email: mishra@ece.ucsb.edu

Grant #: FA9550-10-1-0069

Program Manager: Dr. Kenneth Goretta and Dr. James Hwang

Air Force Office of Scientific Research – Terahertz Electronics Program

1. Abstract

Wafer-bonded current aperture vertical transistors, BAVETs, are a novel approach to obtaining high frequency switching and breakdown. Transistor functionality has been obtained for such devices, but certain challenges, like high saturation voltages, on-resistance and low channel breakdown, have limited the performance. It is argued that performance anomalies arise from the trap behavior of specific region in a BAVET, and that is the wafer-bonded interface (WBI). In an experiment that passivates traps at WBI, an elimination of the anomalies in a BAVET is achieved. Specifically, its saturation voltage and drain resistance are lowered and critical field to impact-ionization is made higher through the optimization of the N-polar InGaN interlayer thickness and the utilization of the p-type III-As gate heterobarrier.

2. Introduction

Electronic devices that employ heterojunctions have improved in various applications such as lighting, energy harvesting and high frequency and power electronics. For instance, they have made light emitting diodes, solar cells more efficient and enhanced frequency and breakdown in transistors [1-5].

A novel heterojunction of InGaAs/Ga(In)N and a vertical transistor design to advancing high frequency power electronics has been proposed in an earlier work [6]. It succeeded in (a) forming the InGaAs/Ga(In)N heterojunction by the method of wafer bonding, (b) providing a basic fabrication technique for a transistor that comprises a wafer-bonded heterojunction, (c) and experimentally showing a partial transistor behavior, which was a promising first step in the development of wafer-bonded electronics. These developments by Snow et al. served a basis for this dissertation's progress.

Fig. 1 shows the timeline of and progress made by this dissertation in advancing wafer-bonded semiconductor transistor technology. The work by Snow et al. was modified in wafer bonding, design and fabrication of the transistor to yield its fully functional DC characteristics (see Fig. 1) [6]. At this stage, however, the properties of

transistor and the related role of wafer-bonded heterojunction or interface (WBI) are scarcely understood. The dissertation attempts to extend this knowledge. Different types of electrical measurements on a varied set of devices and experiments are performed for understanding both transistor and WBI performances (see Fig. 1). The data is analyzed and statistically correlated to isolate key device physics and phenomena. In this process the dissertation deduces certain fundamental properties pertaining to WBI and transistor and establishes methods to enhance their performance (see Fig. 1).

3. Motivation Behind Wafer-Bonded Transistors

3.1. Transistors by Heteroepitaxy

Research in transistor development has been mainly motivated by the demands of higher operational frequency, as well as voltage in electronic applications. Development in epitaxial methods has enabled formation of transistors comprising heterojunctions like AlInAs/GaInAs, and AlGaN/GaN. The use of a heterojunction has enhanced the performance and design space of transistors. Band engineering in an InP-based heterojunction bipolar transistor (HBT) has been shown to yield enhanced current gain and operational frequency [4]. Whereas in the case of a high electron mobility transistor, a heterojunction induces a channel comprising 2-dimensional electron gas (2DEG) and provides the band offset for gate-modulation of the 2DEG [7] (see Fig. 2). The performance benefits are depicted in Fig. 3 (a), wherein InP and GaN-based heterojunction transistors are able to switch at a higher frequency and breakdown voltage than those comprising Si.

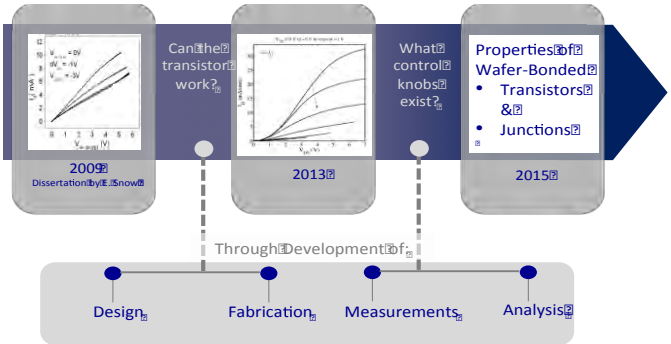


Fig. 1. A flow chart diagram represents the timeline and stages of this dissertation work. An initial work by Snow et al. yielded a wafer-bonded transistor characteristics shown in the first frame [6]. This study extends on that work and modifies transistor's design and fabrication methods to enhance the DC performance. A fully function transistor behavior is obtained and is shown in the middle frame. The latter part of this work deals with correlating and analyzing different types of measurements to deducing the mechanisms and electrical properties of wafer-bonded transistor and junctions.

By exploiting the polarization properties of the III-N system, both Ga- and N-polar based III-As/III-N wafer-bonded transistors are being developed. Specific to its unique device-design and layer-structure, there is a huge design space that needs to be explored and understood to fully exploit the potential of this device-technology. And only a small part of this design space is presented. Herein, we discuss the progress and current status in the development of $In_{0.53}Ga_{0.47}As$/(In)GaN-based wafer-bonded electronic devices.

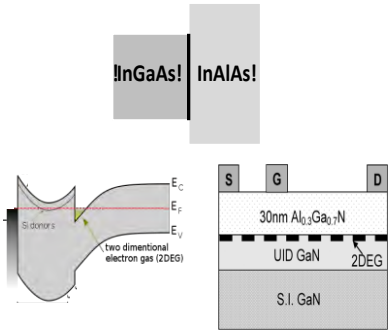


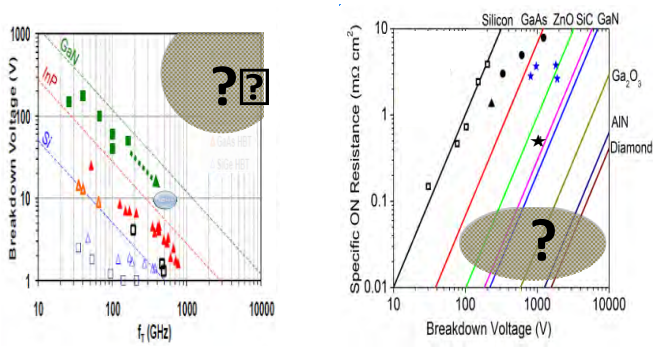
Fig. 2. An example epitaxial InGaAs/InAlAs heterojunction is shown, wherein InAlAs is a wider bandgap material than InGaAs. (b) An energy band diagram of a doped InAlAs/InGaAs junction is shown to highlight 2DEG formation in InGaAs. A 2DEG channel is a fundamental advantage in a high electron mobility transistor (HEMT). A HEMT's schematic is shown in (c) which is based in III-N material system and comprises an AlGaN/GaN heterojunction.

3.2. Wafer-Bonding to Enhance Performance of Transistors

The development of transistors in a material system is determined by theoretically derived roadmap of frequency or on-resistance vs. breakdown (see Fig. 3) [8], [9]. A common attribute that is reflected in such roadmaps is that a gain in operational frequency or reduction in on-resistance is made possible at the expense of a reduction in the highest operable voltage, and vice versa. Thus, the development is stifled by the limits set by the choice device design and material system.

As shown in Fig. 3, InP based high electron mobility transistors (HEMTs) [10] and heterojunction bipolar transistors (HBTs) [4] dominate the applications requiring near-terahertz switching operation. On the opposite hand, GaN-based transistors have demonstrated enhanced output power in the sub-terahertz regime [5]. Thus, integrating

these two distinct material systems in a transistor is a promising approach to further improving power switching operation at ultra-high frequencies.



(a) (b)

Fig. 3. Breakdown voltage vs. (a) current-gain cut-off frequency (f_t) and (b) on resistance trends is shown for different semiconductor technologies [8], [9]. Each technology's development follows a slope that presents a trade-off in between breakdown and f_t or on resistance. The circled region illustrates the untapped performance potential in transistor design. And whether a THz power transistor is achievable by a wafer-bonded transistor based on both III-As and III-N material systems is the motivation behind this work.

The challenge opens up an opportunity of exploration in choosing more than one material system and combining them into one structure for the transistor. In such a transistor, the trade-off arising from material limit placed by a material system on a parameter, such as breakdown voltage in InP-based system, can be avoided in the following manner. If an InP-based transistor incorporates a second material system, such as GaN, which supports higher breakdown limits, then the trade-off can be overcome. An III-Arsenide (III-As)/III-Nitride (III-N) transistor is a promising candidate to simultaneously achieve the two figures of merit of frequency or on-resistance and breakdown in a transistor (see Fig. 4).

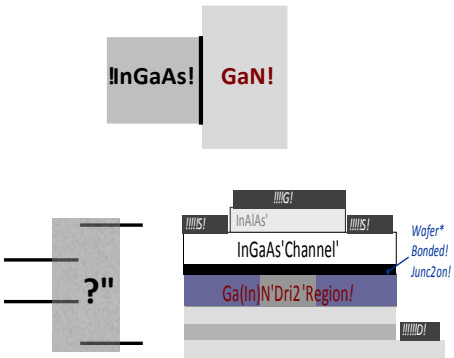


Fig. 4. The study focuses its investigation on InGaAs/Ga(In)N junctions, the properties of which are less known. Additionally a novel III-As/III-N transistor comprising this junction and its properties are proposed and demonstrated.

Investigations may then start by forming a heterostructure comprising both III-Arsenide (III-As) and III-Nitride (III-N) material systems. But such formation is difficult to achieve by means of currently available epitaxial methods, as these are limited to

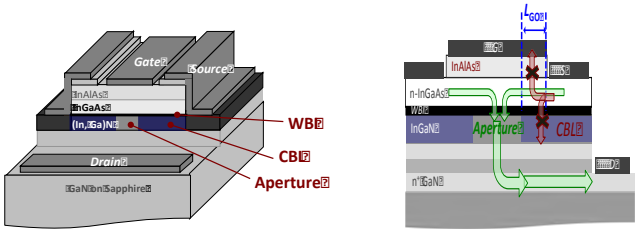
materials systems that are close to similar in their crystal properties. An attribute made absent by widely dissimilar crystal structures and lattice parameters between III-As and III-N materials. Epitaxy is thus not suited for forming a III-As/III-N transistor structure but is achievable by an enabling technology called wafer bonding [11].

3.3. Wafer-Bonded Transistor - BAVET

A III-As/III-N structure can be fabricated into a transistor. A special case of wafer-bonded transistor arises when a transistor comprises of channel derived from a material system different from the one that contains the drift region.

The purpose is served in a type of wafer-bonded transistors called wafer-bonded current aperture vertical electron transistor (BAVET). A BAVET has its design based on principles of a CAVET [12] with certain exceptions. Like a CAVET, a BAVET also comprises of gate-barrier, channel and a drift region with aperture and CBL (see Fig. 5 (a)). A part of the device's active region comprises of an interface, named wafer-bonded interface (WBI), which is what makes BAVETs unique from CAVETs (see Fig. 5 (a)). The interface is named such, on account of its formation through the process of wafer bonding.

Introducing InGaAs/InGaN wafer bonding in a CAVET structure helps meet the following two intentions: (a) an InGaAs channel to provide a high mobility or high injection velocity transport of the current-carrying electron, (b) that is collected in a drift region of wider bandgap GaN-based material capable of withstanding high electrostatic fields.



(a) (b)

Fig. 5. (a) A 3-dimensional view of a BAVET is shown. Among its features are an InAlAs layer acts as a gate-barrier to a channel in InGaAs and the stack of InGaN, GaN layers provides for drift region. InGaN layer is ion implanted in selected regions referred to as the current-blocking layer or CBL regions. The region in InGaN that is disposed between the two CBL regions is referred to as the aperture. Aperture and CBL are features that implement the vertical topology of the device. WBI is an additional feature added by the process of wafer bonding. (b) A cross section schematic of a BAVET showing the gate-modulated L_{GO} regions of InGaAs. Gate-modulation happens on account of current blocking in directions towards InAlAs and CBL barriers in L_{GO} regions, which is denoted by crossed-out arrows. A second set of arrows mark the conduction path of electrons from the source contact to the drain-contact, through the L_{GO} regions of the channel, WBI, drift region and terminating at drain electrode.

Operation of a BAVET is initiated at the source contact with the injection of electrons into n-doped InGaAs. The electrons transit laterally through InGaAs, which is sandwiched between InAlAs and CBL (see Fig. 5 (b)). InAlAs and CBL layers create a barrier to electron in the direction of both gate and drain respectively. Applying bias voltage to the gate controls the channel conductivity in the L_{GO} regions (denoted by L_{GO} in Fig. 5 (b)). Once the electrons exit the L_{GO} region, the applied drain voltage pulls them towards an n-doped InGaN aperture. Electrons enter InGaN aperture from InGaAs, through the WBI. The transit of electron in the vertical direction is confined to the aperture by the presence of CBL-induced barriers on either sides of the aperture. The electrons transit through the drift region and are collected at the drain-contact. Aperture and CBL together implement the function of transporting only the gate-modulated electrons from the source contact to the drift and so are critical for transistor's saturation and pinch-off.

The operation described herein is similar to CAVET but the role of WBI in that of a BAVET is understood and presented in detail in the course of this work. It finds WBI to be a key feature that determines both operation and performance of a BAVET.

4. Scope of This Work

One of the intentions of this dissertation is to experimentally realize near ideal behavior in a BAVET and WBI (see Fig. 1). Identifying and report the key properties of the two is another goal of this dissertation (see Fig. 1).

The work addresses the first goal of establishing the fabrication process of a BAVET and its design of aperture and CBL regions, respectively. The first DC transistor operation is demonstrated.

Anomalies in BAVET characteristics are identified and the underlying properties are deduced. Anomalies are proved to arise on account of parasitic effects, for instance, virtual gate effect, and low critical field to impact-ionization of WBI.

The study leads to identification of trap-affected WBI as the anomaly-causing feature of a BAVET and reports a method that modifies trap behavior of WBI and consequently BAVET's characteristics. Experiment results in a nearly trap-free WBI and anomaly-free

BAVET characteristics, which are the two major performance enhancements achieved by this work.

Historically, growing high-quality N-polar III-N has been recognized to be much more challenging than its Ga-polar counterpart. One of the key challenges has been the formation of hexagonal hillocks on its surface. Therefore, the development of N-polar III-N based devices was initiated later than Ga-polar III-N based devices. With the success achieved in growing high-quality N-polar III-N, we were able to start developing the N-polar III-N based BAVETs.

5. Design Of a BAVET

Can a unipolar wafer-bonded transistor, BAVET, function as a transistor? If it works as a transistor then does it suffer from any abnormalities in its performance? What are the key features that not only make the transistor work but also make it work without anomalies. These are some of the questions answered in this work.

In designing the aperture and current blocking layer (CBL) of a BAVET, one may find the answer to the first question. The abnormal nature in a BAVET if originates at the wafer-bonded interface (WBI), then designing for a well behaved WBI may hold the key to a well behaved performance in a BAVET. So the second question may be answered. In answering these two questions, the study also reveals information on the third unknown. Designing aperture, CBL and WBI, may be tightly coupled to dramatic improvements in the performance of a BAVET and therefore they may well be the features that yield a BAVET. The study presents three experiments, each pertaining to a feature.

5.1. Introduction To Design Of Aperture and CBL

A vertical transistor of the form of a CAVET functions as a transistor on account of the presence of CBL and aperture [12]. A channel carries the current laterally and an aperture does it vertically. To set a current path such as this, it is necessary that a current-blocking layer (CBL) be present in regions below the channel and around the vertically conducting aperture (see Fig. 6). The conductive aperture and blocking CBL end up becoming different regions of a semiconductor layer. The challenge lies in obtaining two regions that are part of the same layer but hold contrasting properties in current

conduction. Aperture must flow as much current that is injected from the channel. A current conducting CBL, on the contrary, unfavorably contributes to leakage in a CAVET. In this work, we are tasked with finding aperture and CBL design for a BAVET, which comprises of a channel in InGaAs; and aperture and CBL in an InGaN layer.

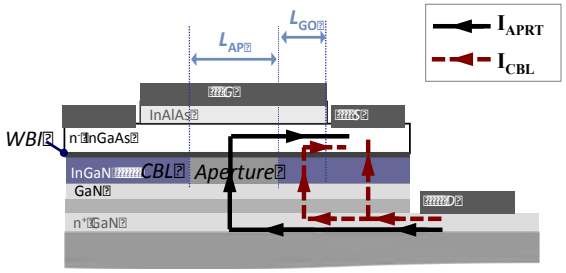


Fig. 6. A BAVET schematic shows the aperture, CBL and WBI. InGaN layer contains the aperture and CBL. InGaAs-InGaN is WBI. Gate barrier is comprised in InAlAs. Current flowing through the aperture and CBL are shown as solid and dashed lines, respectively. G, S, D denote the gate, source and drain electrodes of a BAVET. Gate overlaps with channel-CBL in L_{GO} region and with the aperture in L_{AP}.

The investigation, starts with explaining the use of n-doping and ion-implantation to design aperture and CBL, respectively. The quality of aperture and CBL can be measured in on current and leakage of a BAVET. Two experiments are conducted: aperture and CBL experiments. Variation to aperture current by n-doping is studied in the aperture experiment. CBL experiment, on the other hand, tests CBLs with different ion-implantation energies for low leakage. Apertures with low and high n-doping concentrations are compared. Highest aperture conductivity, or current, is obtained if the doping is high and δ-doped at an interface between the InGaN and GaN layers. A relationship between polarization of III-Nitride region of the BAVET and its aperture conductivity is illustrated.

CBLs are fabricated and tested for a range of ion-implantation energies between 20 and 63 KeV. Only 53 and 63 KeV CBLs show lowest leakage. An explanation of this outcome is posited. Due to the change in the nature of point defects, in ion implanting at one or the other energy, differences are observed in leakage characteristics of different CBLs. High energy CBL and δ-doped aperture are found to be the two necessary conditions towards low turn-on voltage, low leakage, high on current and, most importantly, a transistor operation in BAVETs.

5.2. Introduction To Design Of WBI

A certain aperture and CBL design obtains us a transistor action in a BAVET. The

performance of which is further improved in another experiment, referred to as the WBI experiment, wherein the doping in the gate barrier layer, InAlAs, is modified. Gate-barrier doping dramatically impacts the three device parameters, namely, turn-on voltage (V_{DS_ON}), saturation voltage (V_{DS_SAT}), and output conductance (G_{OUT}). The phenomenon is unrelated to change in channel conductivity but arises from a change in behavior of InGaAs-InGaN WBI. The experiment brings out an interesting fact that a doping in a layer, which is the gate barrier that is remote to WBI, has a dramatic influence on the electronic properties of the latter. This improvement in WBI behavior eliminates anomalies in a BAVET and so makes it well behaved in multiple device parameters.

The three experiments on aperture, CBL, and WBI are interrelated. For instance, the most conductive aperture from the aperture experiment is chosen for the BAVETs studied in the CBL and WBI experiments. Therefore, in the description of each experiment is contained not only the design changes, but also its results and discussion.

6. Methods To Design And Characterize Aperture And CBL

6.1. Aperture Conductivity by n-Doping

For InGaAs/InGaN BAVETs discussed herein, aperture and CBL reside in the InGaN layer. n-doping the InGaN produces the conductive nature in apertures and on changing the dopant concentration, the aperture conductivity is varied. The decisions on doping concentration and what region of the layer is to be doped rely on magnitude and location of a barrier, if it exists, that inhibits electron flow. A barrier may arise as a consequence of the polar nature of the III-Nitride, especially that of the InGaN-GaN interface (see Fig. 6).

The two ends, one that is next to InGaAs and the other to GaN, are the Gallium- and Nitrogen-faces of InGaN layer, respectively. These faces are bound to oppositely ionized polarization charges. These charges, if uncompensated, produce electrostatic field that either aids or works against the one due to a doped junction [13]. Therefore, polarization at the interfaces needs to be considered in choosing the concentration and position of n-doping for an aperture.

Once InGaN is doped for aperture, CBL regions may be formed. As recalled from the earlier section, CBL is, by name and principal, a region whose conductivity should be as low as possible. How to form a CBL is the subject of next section.

6.2. Ion-Implantation for CBL

Countering n-type conductivity by ion implantation is an effective method to create CBL [12]. For a given target layer, the strength of current blocking may depend on a number of factors ranging from conditions like type of ion-implantation ion dose, and energy [12], [14]. The conditions that were previously deduced for GaN in CAVETs act as a sound basis to the study of finding those suited for InGaN layer of BAVETs [15].

The study follows ref. [15] in the choice of the type of ion and the ion-implantation dose, namely aluminum ions [Al^{+}] and 10^{15} cm^{-2}, respectively. The energy of ion-implantation is adjusted based on the difference in the In composition, the thickness and n-doping of an InGaN layer of a BAVET, and that of a GaN layer in a CAVET. This study characterizes a range of energies as InGaN CBL.

6.3. Device Parameters impacted by Aperture and CBL

It is necessary to center the investigation on those parameters of a BAVET that are directly impacted by the properties of aperture and CBL. Conversely, the quality of the two can be evaluated by the value exhibited for certain parameters of transistor.

Aperture Conductivity and On-Current

The current density available from the device depends on how conductive is the aperture. An explanation of the connection follows. Fig. 6 illustrates that the current, I_{APRT}, on exiting the channel is carried in the aperture. Under on state conditions, the InGaAs channel is not fully depleted, and so is not current limiting. But I_{APRT} may be limited in the aperture region if there is a barrier or resistance. Therefore, in having a conductive aperture, a BAVET is able to operate at high on state currents. In a latter section of the study, aperture with different conductivity will be compared by the I_{APRT} measured for a given drain voltage.

CBL Current as a Leakage

With regards to CBL, transistor functionality is compromised if CBL is leaky. Let us

briefly discuss how this happens. CBL is principally the back-barrier for channel with a function of blocking leakage currents. A low barrier has an undesired outcome of electrons transiting unhindered from source-electrode to channel, and into the drain electrode, through CBL. Fig. 6 shows leakage currents, I_{CBL}, in L_{GO} and access regions of the device. I_{CBL} is a parasitic current flowing in parallel to I_{APRT} and determines gate-control on the channel.

Gate Control in a Transistor

Gate control in a transistor refers to a mechanism by which an applied gate voltage regulates the channel depletion width and thus, its conductivity [16]. Two key functionalities of a transistor depend on the gate-control. Pinch off of the channel at its drain edge causes the current saturation and that at the source edge aids in switching off the device.

CBL Leakage and Gate Control in a BAVET

I_{CBL} impacts a BAVET in its gate-control. A leaky CBL unfavorably gets rid of the two functionalities in a BAVET. It cannot pinch-off in either case, for the electrons from the source may escape through the back-barrier in both the L_{GO} and access regions (see Fig. 6). In measuring source-drain leakage through CBL and/or transconductance (g_m) in a BAVET, the blocking attribute of a CBL is tested.

7. Structure and Layout of BAVET

7.1. III-N Layer Structure

The InGaN and adjacent GaN are the two layers that are modified in the aperture and CBL experiments. The remaining III-Nitride (III-N) and the III-Arsenide (III-As) layers are similar to those described in an earlier study [17].

InGaN layer is grown as thick as 50 nm, and can be doped n-type. The layer can be considered as one wide aperture; L_{AP} extends from one edge of the wafer to another. This wide aperture is modified into many narrow ones by selectively ion-implanting the InGaN layer. Ion implanting InGaN in some regions while protecting it in other parts by a metal mask achieves the selectivity. Regions underneath the mask are narrow apertures,

and those without it become CBL. The mask is removed prior to wafer bonding. BAVETs are fabricated on wafer-bonded III-N/III-As stack, with III-N comprising aperture and CBL [17].

7.2. What L_{AP} to choose?

One can either choose BAVET or diode structures for the measurement of I_{APRT} and I_{CBL}.

I_{APRT} and I_{CBL} are measured in BAVETs that differ in their L_{AP} and are biased in the manner shown in Fig. 7. I_D-V_{DS} traces are measured while the gate-electrode is kept open. I_{APRT} becomes the current conducted between the source and drain electrodes of a BAVET, which has an L_{AP} that is chosen in a range of 3 to 15 μm (see Fig. 7 (a)). Source-drain current if measured for L_{AP} = 0 μm represents the current permitted by a CBL, or I_{CBL} (see Fig. 7 (b)). I_{APRT} and I_{CBL} can, additionally, be characterized on two-terminal diode structures comprising aperture lengths greater than and equal to zero, respectively.

8. Experiments, Results And Discussion

The changes in I_{APRT} and I_{CBL} of BAVETs effectively track changes in the conduction properties for different aperture and CBL designs. Those that exhibit the highest I_{APRT} and the lowest I_{CBL}, become the preferred choice for aperture and CBL.

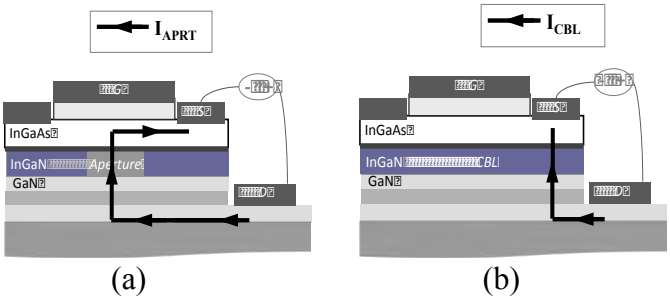


Fig. 7. Two types of BAVET structures are shown with (a) a non-zero, and (b) a zero L_{AP}. For each device, both source electrodes are grounded while the drain electrode is positively biased. The current paths are shown for one of the source electrodes. BAVETs in (a) and (b) yield I_{APRT} and I_{CBL}, respectively. I_{APRT} is the desired current while I_{CBL} is a leakage in BAVET.

8.1. Aperture Experiment

Experiment: Different n-doping concentrations for InGaN and GaN layers

The experiment varies the doping in the bulk of InGaN, GaN layers and their interface. Three doping schemes are proposed. In two, the layers are uniformly doped over their respective thicknesses. In one such case, referred to as low-doped scheme, InGaN is n-doped at 8×10^{17} cm^{-3} and GaN at 3×10^{17} cm^{-3} (see Fig. 8 (a)). These concentrations are increased by an order of magnitude for the second doping scheme named as high-doped (see Fig. 8 (b)).

The layers can be selectively doped to comprise of both high as well as low-doped regions. This is achieved in a third type of doping scheme in which the InGaN-GaN interface is δ-n-doped as the bulk of the InGaN and GaN layers are maintained at low n-doping (see Fig. 8 (c)). Such a structure is hereinafter named δ-doped.

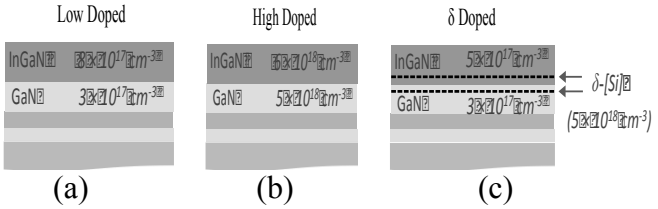


Fig. 8. Three III-N structures for the aperture experiment are shown. (a) Low doped, (b) high doped and (c) δ-doped structure. Each structure differs in their doping of InGaN and GaN layers.

The three structures for the aperture experiment can analogously be described by the statement that a low-doped structure differs from high and δ-doped in the doping of the InGaN-GaN interface. These three structures are processed to yield BAVETs, referred to as low, high, and delta doped BAVETs. These are characterized by I_D-V_{DS} measurements.

Results: I_{APRT} vs. Doping

On varying the doping from low to high, or δ-doping, there is a marked difference in I_D-V_{DS}, which is in contrast to that between high and δ-doped devices (see Fig. 9). For an applied voltage of 4 V, I_{APRT} for δ-doped or high-doped aperture exceeds the low-doped aperture by 5 orders of magnitude. Conversely, the turn-on voltage is lowest for δ- and high-doped apertures. These two designs are so well suited for aperture.

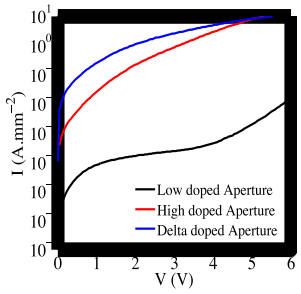


Fig. 9. The I_D-V_{DS} or I_{APRT}-V_{DS} measurements are shown for different types of aperture. I_{APRT} is scaled by aperture's area. Low doped structure yields lowest I_{APRT}. The apertures have a width of 75 μm. L_{AP} is 10 μm for low and high doped; and 4 um for δ-doped aperture.

Discussion: InGaN-GaN interface and its Polarization

From an earlier section one can recall that in low-doped structure interface is low doped while in the other two it is doped high. The difference in I_{APRT} for different doping is a result of the difference in the doping of InGaN-GaN interface. We proceed to explain the mechanism by this relation is brought about.

Polarization effects at the interface may need to be considered. For Ga-polar InGaN-GaN homojunctions, piezolelectric polarization causes a net negative charge at the interface [13]. Reciprocal space map measurements for the III-N structure shows that the InGaN layer is fully strained to GaN layer. The result of such strain is piezoelectric polarization and a net negative charge at InGaN-GaN interface. Negatively ionized charges, if uncompensated, deplete n-doped layers on either side of interface. Depletion electrostatics creates a barrier in the conduction band. It is this barrier, referred to as Ψ_{bi}, that appears in a low-doped aperture, and unfavorably blocks electrons, and so limits current, or I_{APRT} (see Fig. 10 (a)). High voltage bias is needed to overcome Ψ_{bi} and therefore, the high turn-on voltage.

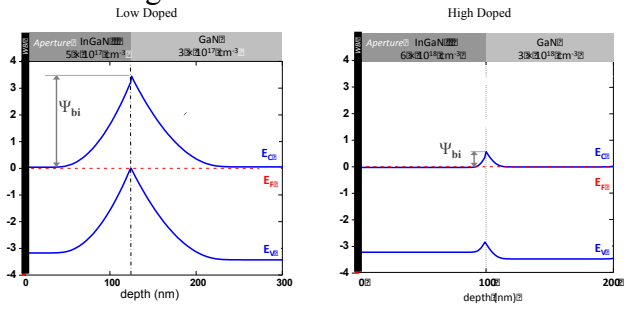


Fig. 10. The layer structure and corresponding energy band diagrams for (a) low and (b) high doped apertures. These are equilibrium band diagrams that are simulated in Bandeng [7]. E_C, E_F, E_V denote conduction band, Fermi-level and valence band, respectively. Ψ_{bi} is the built-in barrier at the InGaN-GaN interface. Simulation shows higher Ψ_{bi} for low doped than high-doped structure.

Doping the interface high, however, compensates the polarization charges through

dopants that are positively ionized. The net interfacial charge is modified such that the higher n-doping, the lower Ψ_{bi} (see Fig. 10 (b)). In the aperture experiment, doping the aperture high, especially at the interface, either by uniformly or δ-high doping, one succeeds in obtaining higher I_{APRT}, and lower turn-on voltage. In understanding the doping dependence of I_{APRT}, the role of polarization on aperture conductivity is hence determined.

The aperture experiment yielded conductive apertures, however, the design for a blocking CBL is yet to be found. For this purpose, we conduct a CBL experiment.

8.2. CBL Experiment

CBLs are, firstly, designed for different ion-implantation energies and then tested for I_{CBL}.

How to choose the ion-implant energies?

In choosing the ion-implantation energy, one has to meet an initial condition that the damage from ion-implantation should be contained within the thickness of target layer. It is well known that the peak position and the width of the ion-implantation profile, called range and straggle, respectively, increase with the energy of ions [19]. In other words, the position of the CBL changes such that it shifts deeper into the stack as the ion-implantation energy increases.

How to fabricate CBLs of low and high ion-implant energies?

Designing CBLs with different energies in a manner that the CBL is contained within a fixed thickness of a target layer is thus a challenge. We address this challenge in two ways. One way is to implant directly into the target layer at energies low enough to keep the damage well within the layer (see Fig 11 (a)). In implant at higher energies, a modified layer stack can be chosen (see Fig 11 (b)). In the modified stack, the target layer is implanted through another layer, called a sacrificial layer. This layer is deposited prior to ion-implantation. The sacrificial layer is etched away post ion-implantation, and what is obtained is a high energy CBL in the intended target layer (see Fig 11 (b)). A larger number of CBLs can be designed this way, as wider range of energies is made accessible.

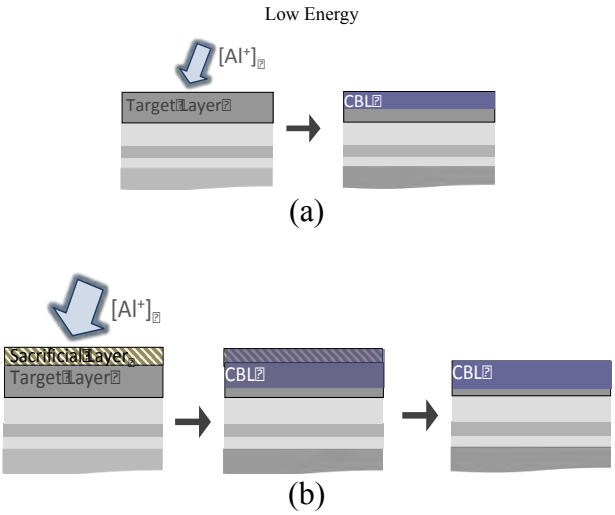


Fig. 11. Ion-implantation layer stack and process are shown for (a) low and (b) high energy CBLs. The two differ in their layer stack by a sacrificial layer, which is needed for high energy CBL. For (a) the process only comprises of ion-implantation step. The ion-implantation step of (b), however, is preceded and followed by deposition and removal of sacrificial layer, respectively. Herein, BAVETs comprise a target layer, which is InGaN, sacrificial layer of Si_xN_y. CBL of low energy depicts that formed at ion-implantation energy 20 KeV, while those that are high energy employ 43, 53 and 63 KeV.

Experiment: Different Energies for InGaN CBL in BAVETs

For the case of ion implanting InGaN without the use of sacrificial layer, SRIM simulation estimates the energy to be 20 KeV [20]. It is the lowest energy used in this study. Any further increasing in energy increases the ion range and so the CBL unfavorably moves from InGaN to the GaN layer.

Depositing a sacrificial layer of Si_xN_y on the top-surface of InGaN layer circumvents the issue. By SRIM simulation, it is found that a 50 nm thick Si_xN_y works well in keeping the ion-range within the InGaN layer. And this holds true for a range of energies between 40 to 60 KeV. Any further increase in energy may require an increase in thickness of Si_xN_y.

Four III-N structures are grown, wherein the InGaN and GaN layers are either doped high or δ-n-type. These doping conditions were deduced by the aperture experiment discussed earlier. One among these structures is ion-implanted at 20 keV using a process similar to that described in Fig 11 (a). In the other three, Si_xN_y is used for the sacrificial layer. For the ion-implantation energy, the three structures are exposed to 43, 53, and 63 KeV (see Fig. 11 (b)). Following ion-implantation, Si_xN_y is removed by a wet etch [12].

Confining ion-implantation profile to InGaN meets only one of the critical conditions in the design of a CBL. There is yet another condition that needs to be met. Do these CBL qualify as layer that blocks I_{CBL}? To this end, the four ion-implanted structures are

fabricated into BAVETs and/or diodes; and characterized for I_{CBL}.

Results: I_{CBL} vs. Ion-implantation energy

I_{CBL} for the four ion-implantation energies is shown in Fig. 12. Lowest I_{CBL} is obtained in those, which have their InGaN layers ion-implanted at 53 and 63 KeV. A significant reduction in I_{CBL} is evident when comparing the I_{CBL} of 43 and 63 KeV. The two differ by six orders of magnitude. The ion-implantation energies to convert an InGaN layer to a current-blocking CBL are hence found to be either 53 or 63 KeV.

The difference of I_{CBL} in 20 and 43 KeV is yet unexplained and needs further investigation. However, we herein attempt on answering the question of why I_{CBL} is such a strong function of ion-implant energy, especially when it is changed from 43 to either 53 or 63 KeV.

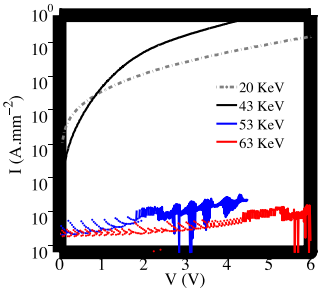


Fig. 12. I_D-V_{DS} or I_{CBL}-V_{DS} measurements are shown for BAVETs differeing in ion-implantation energy. I_{CBL} is scaled by area of the source electrode. It has a width of 75 μm and a length is 15 μm. 53 and 63 KeV CBLs flow the lowest I_{CBL}.

Discussion: Mechanism by which current-blocking depends on ion-implant energy

A hypothesis is presented for the mechanism behind the current-blocking nature of an ion-implanted region or CBL. In an n-doped InGaN layer, before it is ion-implanted, the Fermi-level is close to conduction band. Ion-implantation creates point defects in the n-doped layer, and so introduces energy levels in the band gap of InGaN. These defect levels can move the Fermi-level closer to the valence band if the following two properties are met. Point defects must be, firstly, not fully compensated by the n-dopants and secondly, associated with energy levels in band gap that are closer to the valence band.

The blocking nature of the ion-implanted layer can then arise from the difference in the Fermi-levels of CBL, which is near valence band, and InGaAs channel. A built in barrier is introduced similar to that in an n-p junction [16]. It is this barrier that brings about the blocking capability in a CBL.

How does the barrier change with ion-implantation energy? The answer to this question can be related to whether the ion-implantation energy changes the distribution of ion-implantation profile or, whether it modifies the nature of point defects.

SIMS on the three ion-implanted structures shows that the implant profile is uniform in InGaN and the ion-range and straggle differ narrowly from one implant energy to another (see Fig. 13). But the similarity in their profiles does not translate to similar blocking properties, especially the leakage current is orders of magnitude greater in 43 KeV CBL than that in 53 and 63 KeV CBLs. It is suggested that a uniformly distributed ion-implant profile in the InGaN does not alone make an effective CBL.

It is then stated that dependence of ion-implant energy and I_{CBL} is due to the former changing the nature of the point defects. The change can be explained by an afore-mentioned hypothesis: point defects, if uncompensated by n-dopants, move the Fermi-level and in doing so they change the conductivity of a CBL.

Ion implanting with 43 KeV or 20 KeV creates point defects that are ineffective to make the CBL a barrier layer. This is attributed to either to n-dopants compensating the point defects and/or by the latter's association with shallow energy levels. The nature of point defects is modified, in their compensation and energy level, on ion-implanting InGaN at 53 or 63 KeV. The low leakage for the two energies, see Fig. 12, implies a presence of a higher blocking barrier in either case. The argument explains how blocking in CBL can be improved by changing the ion-implant energy. However, further experimental proof in support of this explanation is required. Photoluminescence measurements may need to be performed for different CBLs in a future study.

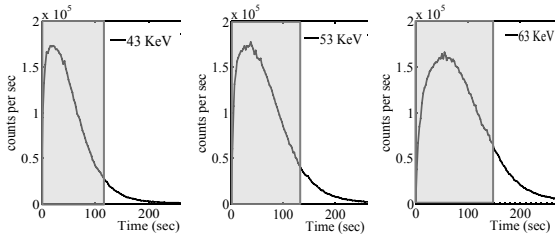


Fig. 13. SIMS profile of Al is shown for InGaN layers that are ion-implanted at (a) 43, (b) 53 and (c) 63 KeV.

In studying apertures and CBLs with different designs and current-voltage characteristics, it is intended that on applying them in a BAVET structure one may obtain a transistor operation. The impact of different designs on the transistor operation is the focus of the section that follows.

9. Transistor Operation In A BAVET

The reason to enhance aperture conductivity and CBL blocking is to realize transistor nature in a BAVET. We are now in a position to test a BAVET for its transistor behavior.

9.1. I_D, I_S-V_{DS}, V_{GS} Characteristics of a BAVET

BAVETs perform poorly to be treated as transistor in the cases whether the aperture is doped low and whether the CBLs are implanted at 20 KeV or 43 KeV. The poor performance is on account of low on current and high CBL leakage, respectively. Only a BAVET, which comprises an aperture that is δ-doped and a CBL that is implanted at either 53 KeV or 63 KeV, exhibits transistor functionality. This type of BAVET works as it is far from being impacted by issues of low on current and leakage. Furthermore, the similar nature of the CBLs of 53 KeV and 63 KeV translates to a similarity that their BAVETs also operate as transistors. Fig. 14 shows the drain (I_D) and source-current (I_S) characteristics of one such BAVET.

An on current of 200 mA.mm^{-1} is obtained (see Fig. 14 (a)). I_S-V_{GS} measurements present a maximum g_m of 55 mS.mm^{-1} at a V_{GS} = -2.3 V. In BAVETs with 63 KeV, maximum on current and g_m, are twice as much at that of 53 KeV. Such increase in implant energy benefits g_m of the device; it is highest for 63 keV and equals 126 mS.mm^{-1}.

9.2. Discussion on Transistor Behavior

Reasons for g_m increasing with ion-implant energy changing from 43 KeV to 53 KeV are understood to be due to the difference in their CBL's blocking ability. But the answer to why g_m becomes twice as much for a CBL changing from 53 to 63 KeV is yet to be found. In explaining the difference in g_m for 53 KeV and 63 KeV, we suspect another phenomenon is at work. As the CBL barrier changes form 53 KeV to 63 KeV, the nature of traps at WBI and CBL region change. The change is such that it increases the channel conductivity and gate-control in L_{GO} regions and thus a higher g_m in BAVETs with 63 KeV. This phenomenon yet needs to be understood in a further investigation.

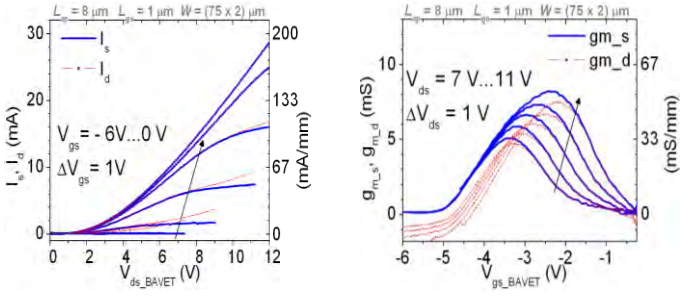


Fig. 14. (a) I_D, I_S-V_{DS}, and (b) I_D, I_S-V_{GS} characteristics measured for a BAVET with δ-doped aperture and a CBL formed by 53 KeV of ion-implantation energy. The difference in I_D and I_S characteristics is due to the gate leakage of device.

9.3. What is not achieved by design of Aperture and CBL?

Although a BAVET is shown to work as a transistor, it yet suffers in performance. Saturation (V_{DS_SAT}), and turn-on voltages (V_{DS_ON}), and output conductance (G_{OUT}) are abnormally high.

The anomalies in each parameter are discussed briefly. (a) Improved CBL design pinches off the BAVET at a threshold voltage (V_{TH}) close to -5 V. V_{DS_SAT}, which represents pinch-off at the drain, however, is greater than 12 V at a V_{GS} = 0 V. V_{DS_SAT} in on-state exceeds V_{TH} by more than 7 V, which is undesirable. (b) Turn-on voltage (V_{DS_ON}) is close to 2.5 V. It is greater than 0 V despite the elimination of InGaN-GaN barrier in δ-doped apertures. (c) Lastly, elimination of CBL leakage improves source-current saturation, and aids in mitigating G_{OUT}, but fails to make it as low as zero.

It is implied that aperture and CBL have a limited role in enhancing the performance of BAVET. It is possible that there exists a third feature that regulates V_{DS_ON}, V_{DS_SAT} and G_{OUT}. The following section presents another experiment to eliminate anomalous nature in a BAVET, and find it's third design feature.

10. WBI Experiment

The experiment is referred to as WBI experiment. It is named so for reasons that will be presented shortly. The experiment comprises designing, fabricating, and characterizing BAVETs with different doping in the gate-barrier or InAlAs layer. The III-N part of the device is unchanged among the BAVETs, and each contains δ-doped aperture and 53 KeV CBL.

10.1. Gate-barrier doping in a Transistor

In a field-effect transistor or FET, gate-barrier has a function of bias modulating the channel. From the theory on a junction FET (JFET), doping of gate-barrier controls the gate and channel potential [16]. Any change to the doping, consequently, modifies V_{TH} and conductivity of the channel in a FET. Likewise, in a BAVET changes in certain parameters with gate-barrier doping are expected.

10.2. Experiment: Changing gate-barrier doping of a BAVET

The gate-barrier of InAlAs is changed in its doping from unintentional to p-type. Two of the structures are referred to as i- and p-structures (see Fig. 15 (a) and (b)). A third structure, referred to as p-i-structure, has InAlAs doped in part as unintentional and in part as p-type. This is done such that the unintentionally doped is sandwiched between the p-doped region and the InGaAs channel (see Fig. 15 (c)).

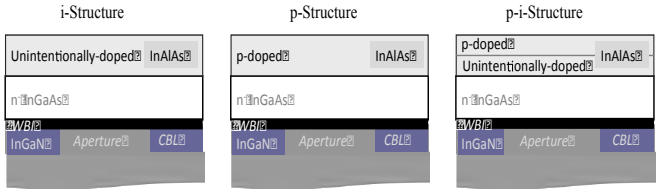
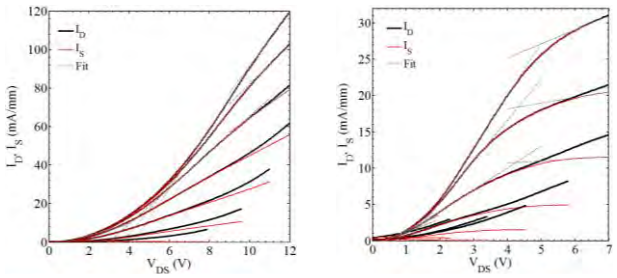


Fig. 15. Wafer-bonded structures that differ in the doping of InAlAs are shown. (a) i-Structure comprises unintentionally doped InAlAs, (b) p-structure with p-doped InAlAs, and (c) p-i-structure containing p-doped InAlAs on top of the one that is unintentionally doped. WBI is the wafer-bonded interface in each structure.

Three III-As structures are grown, wafer-bonded to similar III-N structures, and processed to form BAVETs [10]. They are referred to as i-, p-, and p-i-BAVET.

11. Results And Discussion

Fig. 16 shows the I_D-V_{DS} traces of a p-i and p-BAVETs. Response of i-BAVET is that shown in Fig. 14 (a). The three BAVETs differ in their I_D-V_{DS} through differences in certain parameters, namely On-resistance (R_{ON}), V_{TH}, V_{DS_ON}, V_{DS_SAT}, and G_{OUT}. What follows is an account of how these parameters (a) are derived and (b) relate to gate-barrier doping.



(a) (b)

Fig. 16. I_D, I_S-V_{DS} measurements are shown for (a) p-i, (b) p-BAVETs. V_{GS} is varied from 0 to -6 V. Linear fitting to different VGS is shown by dashed lines. Linear fitting is used to extract V_{DS_ON}, V_{DS_SAT}, R_{ON}, G_{OUT} [10].

11.1. Finding Medians of Device Parameters

I_D-V_{DS} traces are linearly fitted to extract R_{ON}, V_{DS_SAT}, V_{DS_ON}, and G_{OUT} [21]. This is identically done to I_D-V_{GS} traces and so is obtained V_{TH}. The median for each parameter is obtained from box-statistic on a set of devices of each type, namely i, p-i, and p-type. In the following section, the trends of median R_{ON}, V_{TH}, V_{DS_SAT}, V_{DS_ON}, and G_{OUT} vs. doping of InAlAs are presented.

11.2. On-resistance and Threshold voltage vs. Doping

In p-BAVETs, higher R_{ON} is observed in comparison to the other two types of BAVETs. V_{TH} experiences a change of 1 V between i- and p-BAVETs. While for i- and p-i-BAVETs, the difference in V_{TH} becomes as low as 0.2 V.

11.3. Turn-on, Saturation Voltages & Output Conductance vs. doping

Box V_{DS_ON}, V_{DS_SAT}, and G_{OUT} vs. InAlAs doping are shown in Fig. 17. V_{DS_ON}, V_{DS_SAT} shown herein are extracted for a V_{GS} of 0 V, which is -2 V for G_{OUT}.

A characteristic is observed which is common to the three trends. Median is lowest if the BAVET comprises p-InAlAs. V_{DS_ON} of 0.97 V, V_{DS_SAT} of 4.48 V and G_{OUT} of 0.73 $mS.mm^{-1}$ are the characteristics of a p-BAVET. The median V_{DS_ON} and G_{OUT} peak in p-i-BAVET, whereas highest V_{DS_SAT} is characteristic to i-BAVET. Similar behavior in medians vs. doping is, too, observed at other V_{GS}.

11.4. Discussion

The doping dependencies in R_{ON} and V_{TH} arise on account of p-doping making the channel deplete [16]. The p-doped layer is closest to the channel in p-BAVETs than in p-i-BAVETs, and so the former experiences most dramatic changes in R_{ON} and V_{TH} from that of i-BAVETs.

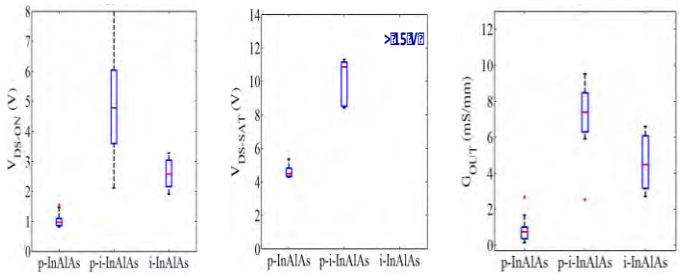


Fig. 17. (a) V_{DS_ON}, (b) V_{DS_SAT} and (c) G_{OUT} expressed in box-plot forms for p, p-i and i-BAVETs. Minima of V_{DS_ON}, V_{DS_SAT} and G_{OUT} vs. InAlAs doping are obtained for a p-BAVET.

R_{ON} and V_{TH} behave in an expected manner with doping but that it also impacts V_{DS_ON}, V_{DS_SAT}, and G_{OUT} is an interesting event. For these are lowest in the case of p-doped InAlAs. It is confirmed that the changes in V_{DS_ON}, V_{DS_SAT}, and G_{OUT} are in response to changes in doping. How doping influences channel, on the other hand, does not explain the connection between doping and the three parameters - V_{DS_ON}, V_{DS_SAT}, and G_{OUT}. Let us briefly explain how the change in R_{ON} or V_{TH} does not translate to similar changes in V_{DS_ON}, V_{DS_SAT} and G_{OUT}. The differences between i-and p-BAVETs are explained.

V_{DS_ON} of i- and p-BAVETs

V_{DS_ON} reduces but not increases with p-doping. This implies that V_{DS_ON} is not due to a barrier in the channel. It neither is from the InGaN-GaN interface, the barrier of which was eliminated by δ-doping. This leaves one region as the possible source of V_{DS_ON}, namely, WBI-aperture region.

V_{DS_SAT} of i- and p-BAVETs

V_{DS_SAT} reduces much more than the observed difference of 1 V in V_{TH} among i- and p-BAVETs. Therefore, the reduction in V_{DS_SAT} is not coupled to p-doping's channel depletion. In another study, it has been found that a virtual gate at CBL-aperture edge of WBI is what cause the difference in V_{DS_SAT} and V_{TH}.

G_{OUT} of i- and p-BAVETs

Between i- and p-BAVETs, the reduction in G_{OUT} is greater than the reduction in on current or enhancement in on resistance. G_{OUT} is, therefore, suspected to reduce due to a reason different from that of channel made less conductive by p-doping. It is proposed that G_{OUT}, in fact, depends on the conductivity of the WBI-CBL interface, which is modified by gate-barrier doping. Further explanation on this subject will be part of another study.

11.5. How to Design WBI in a BAVET?

Detailed accounts of V_{DS_ON}, V_{DS_SAT}, and G_{OUT} vs. doping are beyond the scope of the present study. However, each parameter is shown to have a relationship to the behavior of those regions that comprise WBI.

Doping in InAlAs influences the properties of InGaAs/InGaN WBI, WBI regulates the performance of the device in more than one way, which leads us to state that WBI is another key feature of BAVETs. The feature is indirectly designed by means of doping the gate-barrier layer. The phenomenon arises in how the doping aids in passivating traps at the WBI. The details of which will be presented in another study. p-doped gate-barrier gains us a WBI that is ideal in its behavior and so obtains a near ideal BAVET.

Three features of a BAVET, namely, aperture, CBL and WBI were the focus of this work. Each feature was understood to regulate specific parameters of the device. The study researched different designs for each feature, and found that only certain designs enhanced device parameters. The improvement led to the improvement in transistor characteristics of a BAVET. Explanations, on why one design worked well in comparison to others, revealed interesting phenomenon in InGaAs/InGaN BAVETs.

12. WBI and its passivation

Junctions by wafer-bonding and their devices can be an alternative to gain performance that is not offered in conventional epitaxy-based junctions and devices.

12.1. Direct wafer bonding

Direct wafer bonding is a technique by which two or more materials can be stacked together with the formation of a heterointerface called the wafer-bonded interface (WBI).

Hereinafter, direct wafer bonding is referred to as wafer bonding. The technique involves taking two semiconductor structures and pressing them against each other at a high temperature (see Fig. 18 (a), (b) and (c)). The result is a wafer-bonded structure comprising two semiconductor layer structures joined through a WBI (see Fig. 18 (d)).

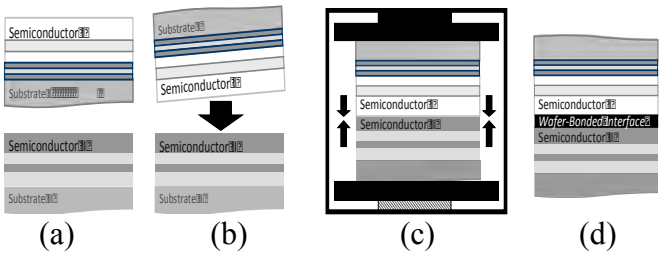


Fig. 18. (a) A cross section of two semiconductor structures on substrate I and II comprising surface layer semiconductor I and II, respectively. (b) A top-down view illustrating the process of placing inverted semiconductor I structure on top of that of semiconductor II. (c) The stack of two structures is placed between two tool plates (denoted by shaded regions disposed on top and bottom of the semiconductor stack) of a wafer bonding system. Pressure is applied to the tool plates (denoted by shaded arrows) such that the two structures are pressed against each other. (d) Cross section schematic of a wafer-bonded structure is shown which comprises a wafer-bonded interface (WBI).

12.2. Need for wafer bonding

Every material system is unique in its physical properties like mobility, bandgap, polarization etc. And these properties can have trade-offs. For instance a material with high mobility can lack in bandgap. III-As provides the former while III-N fulfills the role of a wide bandgap material. A structure comprising both III-As and III-N materials is therefore well suited to make a THz transistor have a large breakdown.

Integrating lattice mismatched material systems by hetero-epitaxy is difficult but if done it leads to the undesirable presence of crystal defects throughout the layer structure [22]. Wafer bonding, on the other hand, opens a space of possibilities in what material structures can be stacked together. It firstly comes without restrictions in lattice constant or crystal nature, and so allows a wider range of material systems to be combined. For instance, integration of $In_{0.47}Ga_{0.53}As$ (InGaAs) and Ga(In)N with a lattice constant mismatch of 46% is made possible by wafer bonding [23], [24]. The extent of defect-rich region may well be limited to a few monolayers of WBI in a wafer-bonded structure, a second advantage in wafer-bonded junctions over heteroepitaxial junctions [25].

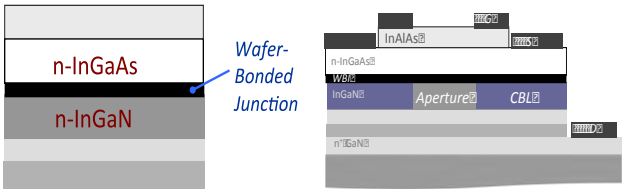
Wafer bonding is widely applied to the device designs of multijunction solar cells, lasers, light emitting diodes (LEDs) and transistors. The operation of these devices requires the WBI to actively participate in current-conduction [26], [27], [28], [29], [30].

The electronic behavior of WBI, thus, plays a fundamental role in achieving the desired operation and performance metrics in the wafer-bonded device.

12.3. An ideal WBI behavior in electronic device

The resultant integration of semiconductors by wafer bonding is prone to defect-formation at the WBI. The impact these defects have on the electronic behavior of the WBI can counteract the desired performance benefits of a wafer-bonded device. Eliminating the undesired trap response has been a challenge for wafer-bonded junctions and has been the main cause of non-ohmic behavior in tunnel-junctions, and limiting the forward-bias currents and impacting the turn-on voltages in p-n junctions. Such deviations from the expected response is attributed to trap-induced Fermi-level pinning or/and trap-assisted tunneling recombination phenomena at the WBI [26], [27], [30], [31], [32], [33]. There is however a lack of information on methods which remedy trap response in wafer-bonded junctions.

Understanding the trap activity of an InGaAs-$In_{0.1}Ga_{0.9}N$ (InGaN) WBI is the subject of this study (see Fig. 19 (a)). It attempts to reduce trap activity, in other words passivate traps, of a WBI. A method to do so is proposed and its applicability in diodes and transistors is reported. Impact of traps is herein studied to rid anomalous behavior in a wafer-bonded current aperture vertical electron transistor, BAVET (see Fig. 19 (b)). It is found that the performance of the devices improve dramatically if their WBI is trap passivated.



(a) (b)

Fig. 19. (a) A cross section of a III-As/III-N wafer-bonded structure showing a WBI between InGaAs and InGaN layers. (b) A cross sectional schematic of a BAVET is shown, wherein InAlAs, InGaAs, III-N region are the gate barrier, channel, and drift regions respectively. Aperture conducts the current vertically while CBL functions as the back-barrier in gate-modulation. WBI interfaces the channel and drift region in aperture and CBL regions. Gate, source and drain electrodes are denoted by G, S, and D, respectively. InAlAs and InGaAs play an additional role in process of passivation of WBI.

13. Role of WBI In A BAVET

13.1. WBI-related anomalies in a BAVET

A WBI in a BAVET is disposed underneath the channel (see Fig 19 (b)). It is an active junction, which interfaces InGaAs to InGaN in aperture and current-blocking layer (CBL) regions. Effects like virtual gate, impact-ionization, drain resistance, have been found to anomalously impact saturation voltage, pinch-off, on-resistance, turn-on voltage, output conductance. It has also been found that majority of these anomalies are local to WBI in either channel-aperture or channel-current-blocking regions of the transistor (see Fig 19 (b)).

13.2. Traps may cause the anomalies

To identify the property of WBI that regulates a BAVET in most of its device parameters and operation, it is necessary that the trap behavior of WBI be characterized and investigated. If the investigation reveals that a method of trap passivation changes trap activity at WBI as well as eliminates anomalies in a BAVET, then it identifies that it is the traps at WBI that control the device performance. It secondly may furnish a proof of the effectiveness of the method in passivating traps.

The study firstly proposes a method to trap passivation, checks its effectiveness in the case of InGaAs-InGaN WBI. It then investigates if the passivation works to improve BAVETs. A description may too be developed with regards to the design BAVETs while considering the role of WBI traps and passivation.

14. A Trap Passivation Method

14.1. Principle of a passivation method

Commonly used techniques to reduce the electrical activity of traps in a semiconductor layer structure, are based on the following two requirements: one of them is the presence of a passivation species, and the other is a mechanism to enhance the migration of passivation species from the region of their origin to the region containing traps. These species can interact with the traps and reduce their electrical activity. The phenomenon of reduction in the electrical activity of traps is referred to as passivation of traps and the species performing this passivation of traps are called passivation species.

Hydrogen, deuterium, fluorine, argon, sulfur may be employed as passivation species during growth or fabrication processes. With regards to passivation techniques, they are

mainly thermal, chemical, or plasma-based treatments of the semiconductor, which incorporate the passivation species and assist in the required migration [34], [35]. In another passivation technique, passivation-blocking layers have been added to the structure to preserve the passivation achieved in a prior thermal-treatment [36].

14.2. Using hydrogen as the passivation species

Growth and fabrication processes can incorporate significant quantities of hydrogen in a semiconductor, and thus the semiconductor can act as a source of hydrogen [37], [38]. Hydrogen can be present in different forms in the semiconductor like isolated hydrogen, a hydrogen molecule and a hydrogen-based complex. Among these forms of hydrogen, isolated hydrogen – hydrogen not bound to any other species, is the most mobile.

In the majority of semiconductors, isolated hydrogen is known to be amphoteric – it can exist either as H^+ or H^- in most semiconductors. H^+ is present when the Fermi level is close to the valence band (or in a p-doped semiconductor) while H^- is stable when the Fermi level is in the upper part of the band gap (or when the semiconductor is doped n-type) [39], [40]. The mobile nature coupled with the charge-switching capability of isolated hydrogen can be used to advantage in trap passivation. Isolated hydrogen can act as the passivation species, which interacts with the trap, consequently results in trap passivation by forming an electrically inactive and stable complex.

14.3. Blocking hydrogen by junction electrostatics

A layer structure may comprise a set of semiconductor-layers, and a trap-containing interface (see Fig. 20 (a)). The latter is named so for its electrically active traps. Passivation species like hydrogen may be incorporated in the layer structure during growth or fabrication processes. The layer containing passivation species is referred to as the releasing layer (see Fig. 20 (a)).

The layer structure comprises of another layer, referred to as blocking layer, which, when disposed in the vicinity of the releasing layer, can provide energy barriers to inhibit migration of passivation species away from the trap-containing region (see Fig. 20 (a)). In other words, increasing the barrier to hydrogen in one direction causes it to move in the opposing direction.

Energy barrier is herein realized in the build-in voltage or junction electrostatics of releasing and blocking layers. Barrier can be adjusted by changing type of dopants and concentration of either layer.

14.4. Thermal process for migrating hydrogen to trap-containing interface

Subjecting the layer structure, which contains the releasing and blocking layers, to thermal processes, can work to enhance the migration of hydrogen (see Fig. 20 (b)). The two layers are disposed in the layer structure such that the migration through the layer structure is enhanced in a direction towards the trap-containing interface (see Fig. 20). Once hydrogen encounters the trap-containing interface, they interact with the traps and results in passivation.

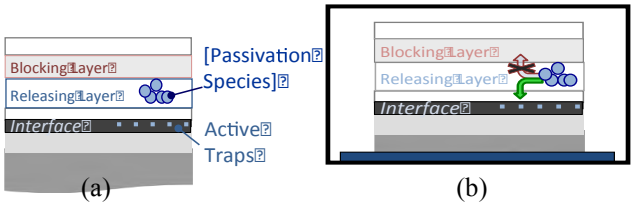


Fig. 20. (a) A schematic illustration of a semiconductor structure comprising an interface with electrically active traps, a releasing layer containing passivation species and blocking layer. (b) The process of passivation during an anneal is depicted. Upward-directed block arrow denotes the blocking of migrating passivation species in the direction towards blocking layer. The downward-directed block arrow denotes the enhanced migration in a direction towards the trap-containing interface.

The layer structure and fabrication can thus be designed with following considerations. (a) Add a releasing layer that is likely to be rich in hydrogen. (b) Sandwich the releasing layer between the blocking layer and trap-containing interface. (c) Choose a doping condition such that the blocking layer provides a higher energy barrier. (d) Lastly, the layer structure may be annealed to aid the migration of hydrogen. The present work develops steps (a)-(d) for an InGaAs-InGaN WBI's trap passivation.

15. Passivating InGaAs-InGaN WBI

15.1. InGaAs as the releasing layer for H^-

A wafer-bonded structure comprising III-As and III-N layer structures is studied. An n-doped InGaAs layer, which is part of a III-As structure, forms a WBI with an InGaN layer of a III-N layer structure. Both III-As and III-N layer structures are grown by

epitaxial techniques (see Fig. 21 (a)) [41]. Hydrogen is unintentionally incorporated during the growth of InGaAs layer, and exists as H^- in the n-doped layer [40]. H^- plays the role of passivation species, and its source InGaAs acts as the releasing layer (see Fig. 21 (a)).

15.2. Doped InAlAs as a barrier layer

Barrier to H^- is too designed in the III-As structure and disposed next to the n-doped InGaAs. A wider bandgap material like $In_{0.48}Al_{0.52}As$ (InAlAs) comprises blocking layer. It's doping and that of InGaAs together determine the electrostatic barrier for H^-. The study seeks the doping in InAlAs that obtains a barrier effective to passivation.

15.3. Thermal process of wafer bonding

The migration process of H^- is thermally activated during the process of wafer bonding (see Fig. 21 (b)). It is performed under vacuum conditions at a temperature of ~ 400°C. A pressure of 5 MPa is applied pressing the InGaAs layer of the III-As against the InGaN layer of the III-N for a period of four hours. The InAlAs-InGaAs barrier provides for an electrostatically driven migration of H^- towards the traps at InGaAs-InGaN WBI and so changes its trap activity (see Fig. 21 (b)).

For a given n-doped InGaAs layer, trap passivation is likely to be enhanced by p-doped InAlAs than that which is unintentionally doped. An experiment is shown herein in which a change of InAlAs doping is performed with the aim of changing or regulating trap activity.

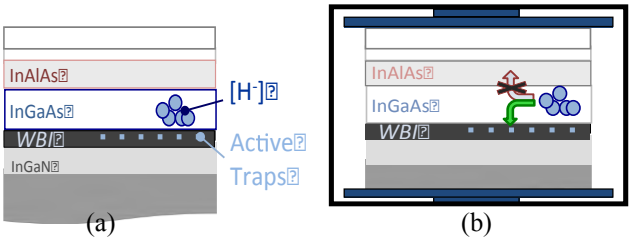
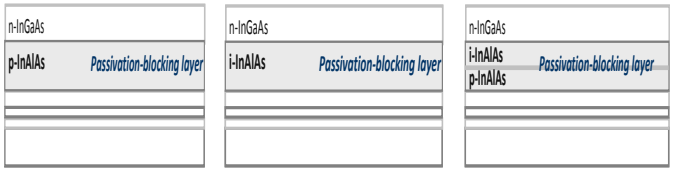


Fig. 21. (a) A cross section of III-As/III-N structure with InGaAs acting as a releasing and InAlAs as a blocking layer. InGaAs comprises of H^-.Active trap region is confined to WBI. (b) An illustration is shown of the passivation process during wafer bonding anneal. The process is illustrated using block arrows marked in the semiconductor structure, wherein one is directed towards the WBI and the other towards the blocking layer (referred to as downward-directed and upward-directed arrows, respectively). Releasing layer of InGaAs releases H-. The downward-directed block arrow denotes the migration of H- in the direction towards InGaAs-InGaN WBI due to barrier from the blocking layer of InAlAs in the direction denoted by upward-directed block arrow.

16. Experiment

16.1. Design three types of barrier layers

Three variations of barrier are studied. Two of which employ p- and unintentional-type doping in InAlAs and are referred to as p- and i-InAlAs, respectively (see Fig. 22 (a) and (b)). For the third variation, which is called p-i-InAlAs, an interlayer of i-InAlAs is disposed between p-InAlAs and n-InGaAs layers (see Fig. 22 (c)). The effective barrier to H- at InAlAs-InGaAs junction decreases in the order of p-, p-i, and i-InAlAs.

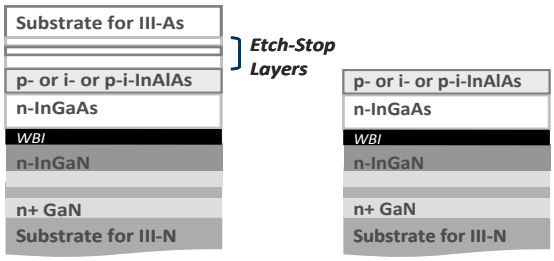


(a) (b) (c)

Fig. 22. Cross section of III-As structures comprising of n-doped InGaAs and three different blocking layer designs: two of the them are designed by doping the InAlAs (a) p-type (denoted by p-InAlAs), and (b) unintentionally (denoted by i-InAlAs). (c) The third design, referred to as p-i-InAlAs, is shown. It comprises an interlayer of unintentionally-doped InAlAs sandwiched between p-InAlAs and n-doped InGaAs. Each structure is inverted and wafer-bonded to III-N structure and tested for differences in WBI trap behavior.

The three types of III-As structures are wafer-bonded to similar III-N structures. A process, which not only creates a WBI but also, enables trap-passivation.

The III-As substrate in each wafer-bonded structure is removed by wet etch to result in a device structure comprising InAlAs, InGaAs and the III-N layers (see Fig. 23). InAlAs and InGaAs, the blocking and releasing layers play additional roles of gate-barrier and channel in a BAVET. While its drift region is comprised in III-N layers (see Fig. 19 (b)). These layers are essential to a device like BAVET [41].



(a) (b)

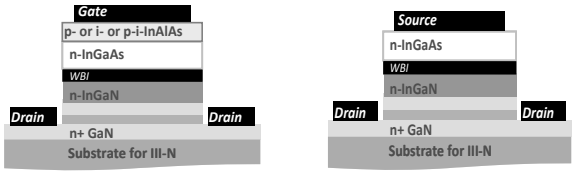
Fig. 23. Cross sections of III-As/III-N structure: (a) after wafer bonding, and (b) after substrate removal, wherein the III-As substrate and etch-stop layers are removed.

16.2. Wafer-bonded diodes and BAVETs to measure a WBI's Trap behavior

Trap-behavior of a WBI can be studied by its electronic-response. For this purpose devices like diodes and transistors are fabricated. The trap-activity of a WBI is deduced from capacitance-voltage (C-V) or current-voltage (I-V) characteristics of diodes and BAVETs.

In order to study trap passivation as a function of InAlAs doping, diodes and BAVETs for each type of InAlAs barrier are fabricated and then characterized.

For a given device structure, diodes can be formed that differ in their contact layers. For instance, contacts if formed to the InAlAs and conductive GaN layer yield a diode referred to as gate-drain diode (see Fig. 24 (a)). A source-drain diode, on the other hand, has its InAlAs layer removed to form one of the contacts to InGaAs layer (see Fig. 24 (b)). The nomenclature is followed in the manner of their relevance to a BAVET (see Fig. 19 (b)).



(a) (b)

Fig. 24. Schematic illustrations of different types wafer-bonded diodes: (a) Gate-drain diode with gate-contact to the passivation-blocking layer of InAlAs and drain-contact to the III-N layer, (b) The passivation-blocking layer is removed from the device structure in (a) to form the source-drain diode, wherein the source and drain-contacts are formed to the passivation-releasing layer of InGaAs and n+ GaN layer. Both the diodes are structurally also differentiated in their electrodes and InAlAs layer. Additionally, InAlAs is doped p-, or p-i- or i-type for gate- or source-drain diodes. InGaN-GaN junction has been delta n-doped to compensate polarization charges. It can be assumed that diode characteristics mainly probe junction electrostatics of InAlAs-InGaN and WBI than InGaN-GaN.

16.3. Trap activity on removing blocking layer after wafer-bonding

It was emphasized that a blocking layer is required during wafer bonding to implement the trap passivation method. But whether trap-passivation achieved during bonding is made ineffective on removal of InAlAs after bonding is yet not known. A test of preservation of trap passivation is needed. Secondly, it is also necessary to isolate whether characteristics of diodes represent trap activity at WBI or that of InAlAs-InGaAs interface.

Both these questions are addressed in experiment that compares trap activity of a diode comprising both the interfaces, namely InAlAs-InGaAs and WBI, to that with a diode that contains only WBI. The latter is obtained by removing the InAlAs layer after

the step of wafer bonding. This not only removes InAlAs-InGaAs interface but also tests its impact on trap passivation of WBI. The purpose is served in a comparison of gate-drain and source-drain diodes.

17. C-V Measurements

Trap activity of WBI is interpreted through C-V and transistor characteristics.

17.1. Capacitance-voltage measurements

The quality of the WBI can be evaluated by performing C-V measurement. It is based on the principle that a change in the applied voltage modulates the stored charge in a semiconductor [38], [39]. Applying reverse bias to a junction diode depletes the stored charge, increases the width of the space charge or depletion region, and leads to a monotonically decreasing capacitance. Increasing depletion width with bias is a consequence of the movement of the Fermi-level across the bandgap with the applied bias. However, C-V trace deviates from the expected behavior when there are trap states in the bandgap as they change their occupancy in response to the sweeping Fermi-level. Additionally, a frequency dependent response in a C-V may arise due to a time constant associated with the traps.

18. Results of C-V Measurements

18.1. C-V as a function of InAlAs doping

Three source-drain diodes are fabricated on the wafer-bonded structures comprising blocking layers of i-InAlAs, p-i-InAlAs, and p-InAlAs (see Fig. 24 (b)). Hereinafter, the three source-drain diodes are referred to as i-, p-i-, and p-source-drain diodes. It should be emphasized that in these source-drain diodes, InAlAs layer is present during the wafer bonding process but is intentionally removed during the fabrication of the diodes. Each of the diode comprises releasing layer, WBI and III-N layers.

With the absence of InAlAs-InGaAs interface, the results of the C-V measurement are expected to be mainly a manifestation of the electrostatics of a WBI. A bias is applied between InGaAs and GaN layers of each of the diode to measure the respective C-V traces. The oscillation signal voltage of 1 MHz is applied.

High-frequency C-V traces of p-, p-i-, and i-source-drain diodes are compared in Fig. 25. Capacitance reduces as p-source-drain diode is biased into the depletion regime. However, in contrast, i- and the p-i- source-drain diodes show an anomalous increase in the capacitance, which is most severe in the former.

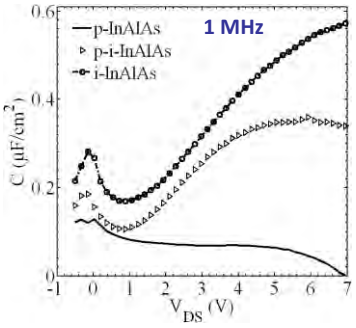
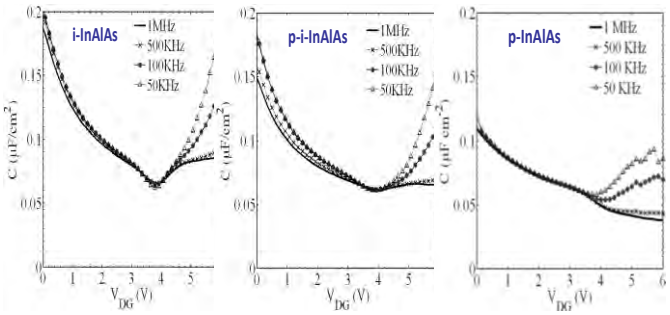


Fig. 25. p-, p-i- and i-source-drain diodes are characterized. High-frequency (1 MHz) reverse-bias C-V measurements of the WBI for each of the diode show Fermi-level pinning in diodes formed from the structures that contained i-, and p-i-InAlAs. Lowest Fermi-level pinning, and thus lowest electrically active trap density, exists in the diode formed from a structure that comprised of p-InAlAs during wafer bonding.

18.2. Frequency-dependence in C-V

A gate-drain diode is characterized for frequency dispersion in a C-V trace. Three types of gate-drain diodes are fabricated from wafer-bonded structures that differ in InAlAs layers. These are referred to as p-, p-i- or i-gate-drain diodes. Unlike the source-drain diodes described earlier, the gate-drain diodes have the blocking layers present in the diode structures (see Fig. 24 (a) and (b)). A bias is applied between InAlAs and GaN layers of each of the gate-drain diode and C-V traces are measured with frequency as the control-variable. The i-gate-drain diode shows a strongest frequency-dispersion in the depletion-regime of the C-V traces (see Fig. 26). It reduces if p-doped InAlAs added like that in a p-i-gate-drain diode. While p-gate-drain diode exhibit the least frequency dependence in C-V.



(a) (b) (c)

Fig. 26. (a), (b) and (c) are the reverse-bias C-V responses of i, p-i-, and p-gate-drain diodes, respectively. C-V is measured as a function of frequency. The applied signal-frequency varies as: 50 KHz, 100 KHz, 500 KHz, and 1 MHz. Frequency dispersion in the depletion regime of C-V is highest for the diode that comprised i-InAlAs during wafer bonding. And the dispersion reduces if a p-i-InAlAs or p-InAlAs are used as the passivation-blocking layer during wafer bonding.

19. Discussion on C-V Measurements

19.1. InAlAs doping influences trap activity of WBI

Incremental trend in the capacitance of i- and p-i-source-drain diodes is observed because the applied voltage is unable to increase the depletion charge but instead charges or discharges the trap states at the WBI. As a result the movement of the Fermi-level is diminished – a phenomenon referred to as Fermi-level pinning. Capacitance increases anomalously as long as the Fermi-level stays pinned. The decreasing trend in the C-V is restored if Fermi-level moves beyond trap states.

The stretch out in C-V behavior becomes higher as well as wider in the order of p-, p-i-, and i-source-drain diodes. Fermi-level pinning is observed to be strongest in i-source-drain diode, which can be attributed to the presence of a larger active trap density at the WBI of i-source-drain diode in comparison to the WBIs in p-i- and p-source-drain diodes.

The WBI of p- source-drain diode which had the highest electrostatic-barrier to H- has, as a result, led to a lowest electrically-active trap density relative to both the p-i and i-source-drain diodes. Additionally, a distinctive trend is observed, wherein a steady reduction in the active trap density at WBI with the increase in InAlAs-InGaAs barrier from i- to p- through p-i-InAlAs. It is proposed that the trap density at the WBI can be passivated by both the approaches, namely: using p-doped InAlAs as well as by the use of an interlayer of i-InAlAs between p-InAlAs and InGaAs layers. The latter is less effective than p-doped blocking layer.

19.2. Improved Trap passivation at WBI of p-doped InAlAs

If on lowering the frequency the depletion capacitance is shifted to higher values and the stretch out in the C-V trace is widened, then it is a proof of a trap-induced Fermi-level pinning as the frequency is lowered. It is so observed for i-gate-drain diodes (see Fig. 26

(a)). The dispersion phenomenon is however mitigated in the C-V of the p-i- and p-gate-drain diodes (see Fig. 26 (b) and (c)). This is another confirmation of the presence of less electrically active traps at WBI when using p-doping and/or p-i-doped InAlAs-based electrostatics to enhance hydrogen-based passivation.

19.3. Trap-passivation unaffected by a post-bonding InAlAs removal

Both p-gate-drain and p-source-drain diodes show reduced trap-induced Fermi-level pinning. Low trap activity is present despite a difference in their layer structure. The passivated nature of the WBI survives the removal of the blocking layer in a fabrication step subsequent to the wafer bonding process. Conversely, it serves the proof that active trap density of an InGaAs-InGaN WBI can be controlled during the thermal process of wafer bonding. Measurement results render the correctness of the argument that hydrogen-based passivation is adjusted by changes to InAlAs blocking barrier and that wafer bonding is the enabling step.

20. WBI in A BAVET

20.1. Operation of a BAVET & role of WBI traps

In a BAVET's on-state operation electrons transit laterally through InGaAs, which is sandwiched between InAlAs and WBI-CBL. Applying gate voltage changes the channel conductivity in the WBI-CBL region (denoted by L_{GO} in Fig. 27). Once the electrons exit the L_{GO} region, the applied drain voltage pulls them towards the InGaN aperture, through the WBI.

On-state saturation and off-state pinch-off in a BAVET are features that are determined by CBL and aperture regions [30], [41]. With a WBI extending over both CBL and aperture regions, the properties of WBI can additionally influence a BAVET's performance.

In a set of studies, to be published elsewhere, transistor characteristics of BAVETs have shown certain anomalous nature in their performance. Those studies have also isolated WBI to be the cause of such anomalies. It is herein argued that if anomalies in a

BAVET are related to WBI's trap-related properties, then in passivating traps one should be able to overcome the limitations in transistor's performance. In the following section, the WBI-passivation method that is developed herein is applied to a BAVET and its results are reported.

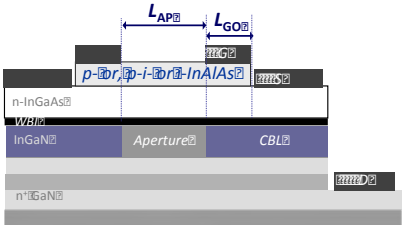


Fig. 27. Cross section schematic of a BAVET is shown. L_{GO} dimension is used to denote the region of InGaAs channel modulated by the gate. The length of aperture is marked by L_{AP}. WBI interfaces the channel and InGaN in both L_{GO} and L_{AP} regions. For this study three types of BAVETs are fabricated that comprise p-, p-i- or i-InAlAs and are referred to as p-, p-i-, and i-BAVETs, respectively.

20.2. Structure of BAVET to study influence of passivation

From the aforementioned discussion on InGaAs-InGaN WBI, it is understood that in the case of a BAVET, the InGaAs channel can be the releasing layer containing hydrogen as the passivation species. InAlAs blocking layer is a gate-barrier. BAVET structure is formed by the wafer-bonding step that also works to passivate WBI.

The experiment of changing InAlAs doping from i- to p-type through p-i-type is also performed for BAVETs. Three types of BAVETs are fabricated, namely, i-, p and p-i-BAVETs (see Fig. 27). Each BAVET is characterized for its I-V_{DS} characteristics and compared with the other to identify the change in I-V_{DS} traces due to the change of trap passivation.

21. Results of BAVET Performance vs. InAlAs Doping

21.1. Transistor I-V characteristics

A WBI is disposed in the vicinity of source and drain edges of the channel of a BAVET. A trap-affected vs. a trap-passivated WBI must yield differences in characteristics of corresponding BAVETs. The results of i, p-i and p-BAVETs are shown herein for the purpose of identifying and understanding their differences.

Fig. 28 shows the source-current (I_S) vs. drain-voltage (V_{DS}) characteristics of three types of BAVETs. Applying p-doped InAlAs improves I_S-V_{DS} characteristics, especially in its current saturation and pinch-off behavior.

21.2. On and off-state performance vs. InAlAs doping

The multiplicity and magnitude of performance changes is classified into device parameters shown in Fig. 28, wherein each parameter is extracted from I-V measurements and plotted against InAlAs doping. Method of extraction is detailed in ref. [21]. A strong dependence of each parameter on the latter is shown. The dependence that may shed light on what causes I-V characteristics to improve in p-BAVETs.

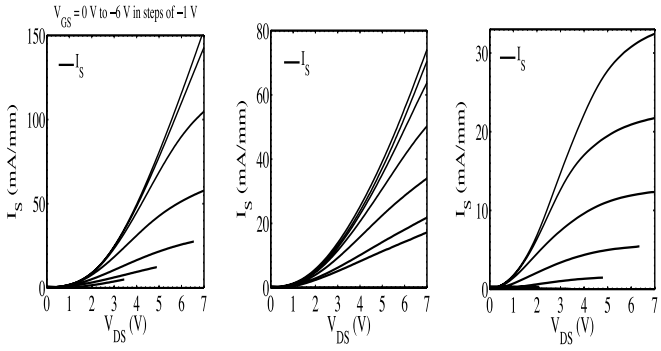
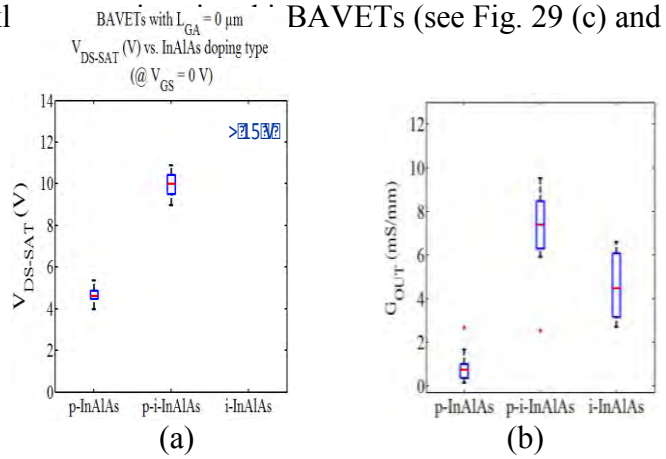


Fig. 28. I_S-V_{DS} traces are shown for (a) i-, (b) p-i-, and (c) p-BAVETs. These are measured as a function of gate-voltage (V_{GS}) varying between 0 V to -6 V, in steps of -1 V. Performance in both on-state saturation and off-state pinch-off is a strong function of InAlAs doping.

Between i- and p-BAVETs, on-state saturation in the former on one hand requires higher V_{DS} (referred by saturation voltage - V_{DS_SAT}) and on the other it is made weak by higher output conductance (G_{OUT}) (see Fig. 29 (a) and (b)). Turn-on voltage (V_{DS_ON}) and drain resistance (R_X) are the other two factors influencing on-state performance. Lower V_{DS_ON} and R_X make a well-behaved I-V trace in a transistor, a feature available for p-BAVETs but weakl BAVETs (see Fig. 29 (c) and (d)).



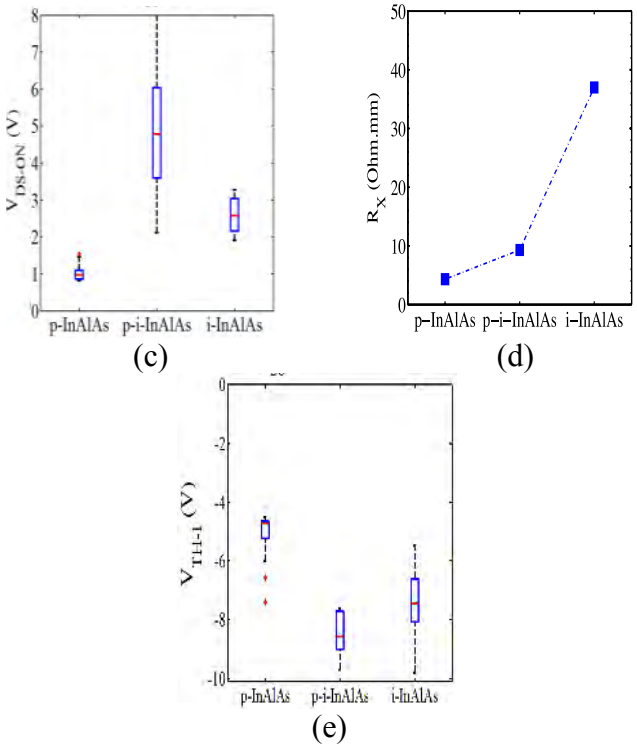


Fig. 29. (a) V_{DS_SAT}, (b) G_{OUT}, (c) V_{DS_ON}, (d) R_X, and (e) V_{TH} are plotted against InAlAs doping. (a)-(c) and (e) are expressed in box-plot forms whereas R_X is represented by median value. These are extracted from I_S-V_{DS} and I_S-V_{GS} traces of p, p-i and i-BAVETs. High anomalous values of these parameters are obtained in i- or p-i-BAVETs. On the contrary, minima of V_{DS_SAT}, G_{OUT}, V_{DS_ON}, R_X, and magnitude of V_{TH} vs. InAlAs doping are obtained for a p-BAVET. The difference in each parameter is not equivalent to changes expected by change of built-in voltage by InAlAs doping.

Obtaining off-state pinch-off is a necessary condition in a transistor's operation and also complements its breakdown characteristics. Threshold voltage (V_{TH}) monitors pinch-off such that if V_{TH} is highly negative then it is likely due to a weak pinch-off. V_{TH} is most negative for p-i-BAVETs and least for p-BAVETs.

It is stated that in i- and p-i BAVETs, the anomalous nature of their I_S-V_D traces arises due to a large set of device parameters being anomalous. In contrast, p-BAVETs respond with a well-behaved transistor I_S-V_D trace mainly because of the absence of anomalies in all of the above-mentioned parameters.

InAlAs doping changes the built-in voltage (V_{BI}) of the InAlAs-InGaAs junction is changed. V_{BI} decreases from 1.47 V in p-BAVETs to 0.7 and 0.53 V in p-i-, and i-BAVETs, respectively. In addition to changing V_{BI}, the doping of InAlAs has been found in this work to also effect trap behavior of InGaAs-InGaN WBI. The question then arises whether it is the InAlAs-InGaAs junction and its V_{BI} or InGaAs-InGaN WBI's trap behavior that changes the nature of anomalies in characteristics of a BAVET.

22. Discussion On WBI Passivation In BAVETs

22.1. Anomalies represent anomalous behavior of WBI

A detailed analysis on V_{DS_SAT}, R_X, V_{TH} vs. InAlAs doping has been presented in ref. [42], [43], and [44], respectively. From the large inequality between how each parameter changes with respect to that expected by the change of V_{BI}, it was hinted that WBI might be the primary factor regulating V_{DS_SAT}, R_X and V_{TH}. Additional deductions were made, namely (a) an anomalously high V_{DS_SAT} is a response of a virtual gate buried in WBI region of BAVETs. (b) The behavior of WBI in the aperture region furnishes the drain resistance of R_X. (c) Critical field of WBI if low can lead to its impact-ionization and so cause large negative values of V_{TH} in a BAVET.

Although the studies arrived at three different phenomena of virtual gate, drain resistance, low critical field, yet it isolated a common feature that the anomalies in device parameters are local to WBI and depend on its properties. What property or properties of WBI regulate the performance of a BAVET are yet not known but reported next.

22.2. WBI Trap Passivation determines BAVET performance

In prior works it was also proposed that anomalous phenomena (a), (b) and (c) of virtual gate, drain resistance, and low critical field, respectively are mitigated for p-BAVETs. But these effects are dominantly present in i- and p-i-BAVETs. Any change to WBI behavior changes the performance of a BAVET.

A high trap activity at WBI of i- and p-i-diodes is identified in an earlier part of this study on wafer-bonded diodes. An increase in trap passivation or reduction in trap activity is also confirmed for diodes with p-type InAlAs. A reduction of trap activity in WBI of diodes if correlated to the reduction of anomalies in WBI of BAVETs suffices new information. It proves that the performance of a BAVET is tightly related to trap-related properties of WBI. Higher the trap passivation of WBI, better the DC and frequency dispersion characteristics in BAVET and diodes.

WBI, a junction formed by wafer bonding between two similar or dissimilar materials, can be prone to the presence of large electrically active trap density. Such trap

behavior was shown to result in poor performance in wafer-bonded diodes and BAVETs. For instance, a high trap activity led to Fermi-level pinning causing high frequency dispersion in diodes. With regards to BAVETs, anomalies in its device characteristics were, too, correlated to trap-related effects of a strong virtual gate, high drain resistance and low critical fields. The study attempted to realize well-behaved diode and transistor characteristics by addressing the trap-related issues of WBI.

23. Development of N-Polar InGaN/GaN BAVETs

The development of N-polar InGaN/GaN BAVETs took the following steps: (1) exploration of N-polar InGaN morphological properties, (2) fabrication of N-polar BAVETs and recognition of their key issues, and finally (3) solving some of those key issues and enabling the BAVETs to be fully functional as a transistor.

23.1. Background of N-polar III-N

Historically, growing high-quality N-polar III-N has been recognized to be much more challenging than its Ga-polar counterpart. One of the key challenges has been the formation of hexagonal hillocks on its surface [45]. Therefore, the development of N-polar III-N based devices was initiated later than Ga-polar III-N based devices. With the success achieved in growing high-quality N-polar III-N, we were able to start developing the N-polar III-N based BAVETs.

The N-polar III-N material – especially with InGaN/GaN layer structure – is inherently advantageous for fabricating BAVETs for two important reasons: (1) there is no polarization-induced barrier at the InGaN/GaN interface in the vertical current path of BAVETs due to the formation of the 2-D electron gas and (2) the surface of N-polar III-N can be prepared ultra-smooth because it is chemomechanically polishable.

Figure 30(a)-(b) compare $In_{0.1}Ga_{0.9}N$/GaN interfaces (with the polarization-induced fixed charge into account) of Ga-polar and N-polar structure, respectively. Unlike the case of Ga-polar III-N in which a huge polarization-induced barrier arises, it is clear in the case of N-polar III-N that the electron that is entering from the InGaN side (left) can smoothly transit into the GaN (right). This makes the N-polar III-N material naturally feasible for fabricating III-As/III-N BAVETs.

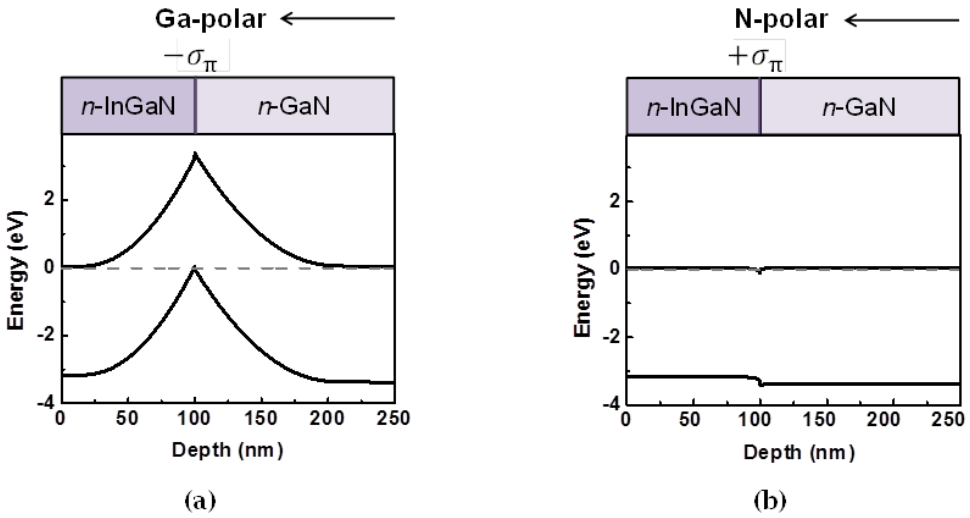


FIGURE 30. Energy band diagrams of (a) Ga-polar and (b) N-polar $In_{0.1}Ga_{0.9}N$/GaN structures taking the net polarization induced charge (σ_π) into account.

Another huge advantage offered by N-polar III-N is its compatibility with chemomechanical polishing (CMP). Figure 31(a)-(b) compare the surface of Ga-polar and N-polar GaN before and after a short 3-minute CMP. The two materials initially have similar surface rms roughness values (as written on the upper left corners). However, after CMP, it is clear that the CMP process does not bring any noticeable effect on the surface of Ga-polar III-N. On the other hand, the surface of N-polar GaN has become extremely smooth with an order of magnitude reduction in its rms roughness. The same effect applies to InGaN surfaces as well. In consideration of wafer-bonding applications, this evidently is another hugely advantageous property offered by N-polar III-N materials. Here, it is noted that we did not utilize CMP for smoothing the surface of N-polar InGaN used for BAVET fabrication, because its layer thickness is quite thin (5-25 nm) – *i.e.* we did not want to polish away all or most of the InGaN layer by performing CMP.

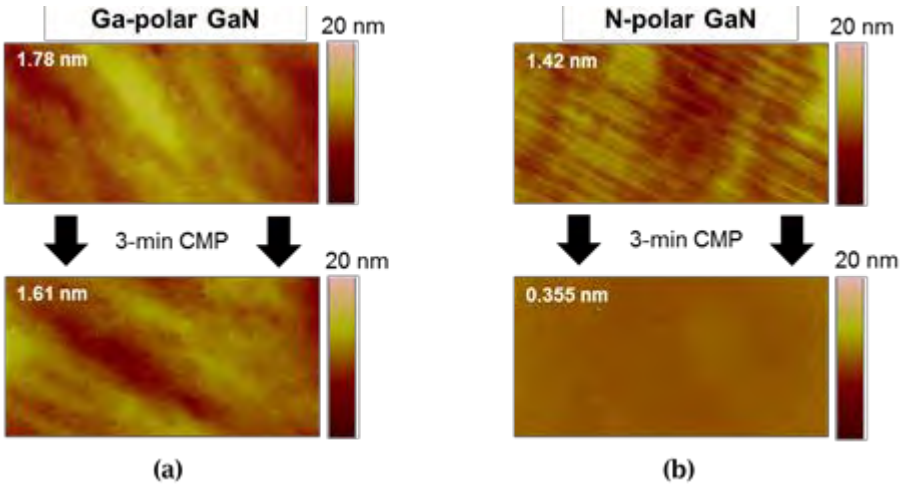


FIGURE 31. 10 μm × 20 μm AFM images of before and after a 3-min CMP on (a) Ga-polar and (b) N-polar GaN. The [nm] value written at each upper left corner is the rms roughness.

23.2. The First Functional N-polar BAVET

After a few generations of development cycles as reported previously, the first functional N-polar InGaN/GaN BAVET was fabricated successfully. Its cross-sectional schematic and output characteristic are shown in Fig. 32(a)-(b). It is immediately observed that the drain current is significantly higher in the N-polar BAVET than the above-mentioned Ga-polar BAVETs. The measured I_D are approximately 100 mA/mm and 540 mA/mm at V_{DS} = 8 V and V_{GS} = 0 V for the Ga-polar and N-polar BAVETs, respectively. This difference can be attributed to the expected benefit offered by the N-polar InGaN/GaN heterojunction, *i.e.* the absence of any apparent barrier to electrons at the InGaN/GaN interface due to its net positive polarization induced fixed charge as discussed above.

Still, the *I-V* exhibits many of the problems identical to those seen in the Ga-polar BAVET, including the presence of a finite turn-on voltage, $V_{DS,sat}$ much higher than the ideal, and very high gate leakage, all of which should be addressed.

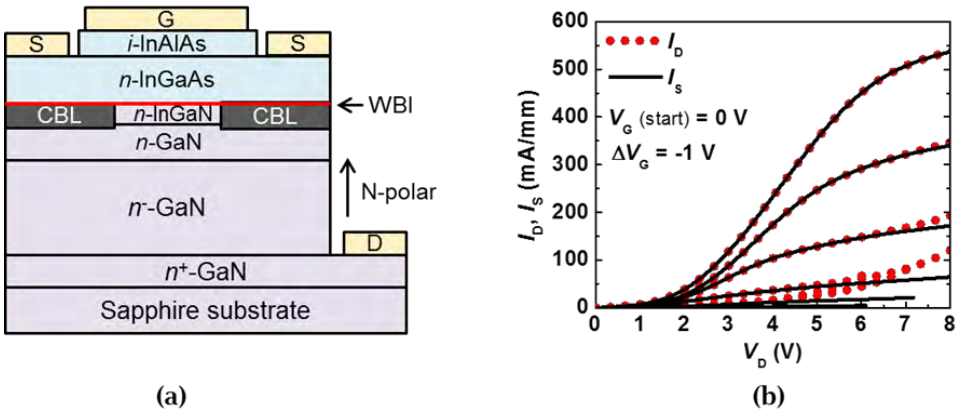


FIGURE 32. (a) Cross-sectional schematic of the first functional N-polar BAVET with an ion implanted, *in-situ* grown 25 nm-thick $In_{0.1}Ga_{0.9}N$ interlayer. (b) *I-V* characteristic of the N-polar BAVET with L_{ap} = 6 μm and L_{go} = 2 μm.

23.3. Addressing the Gate Leakage in N-polar BAVET

For this study, we have utilized the doping series of the gate heterobarrier material (InAlAs) as previously shown in Fig. 15(a)-(c). Because of the introduction of p-type InAlAs in the cases of Fig. 15(b) and 15(c), it is predicted that the gate leakage should reduce with increasing p-doping and/or thickness of p-InAlAs layer.

Because the higher electron barrier introduced by p-InAlAs also means the effective channel thickness is decreased, we can also expect to see a reduced maximum current in the case of p-InAlAs containing BAVETs for transistors with identical n-InGaAs channel properties.

The results of BAVETs fabricated with the three different gate heterobarriers are shown in Fig. 33(a)-(c). It is observed that the maximum drain current is decreasing as a thicker p-InAlAs (0 nm to 20 nm to 50 nm from (a) to (c)) is introduced in the heterobarrier, which was expected. However, the expected gate leakage reduction was not noticeably observed from the p-InAlAs based BAVET.

On the other hand, by closely observing the *I-V* characteristics, it is observed that the turn-on voltage as well as the $V_{DS,sat}$ are reducing with the introduction of thicker p-InAlAs gate heterobarrier.

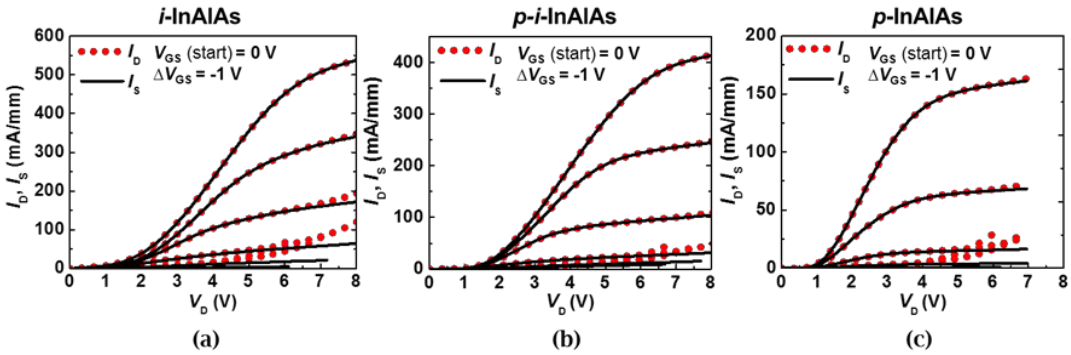


FIGURE 33. (a) Measured output characteristics of BAVETs with (a) 50 nm-thick i-InAlAs, (b) 20/30 nm-thick p-InAlAs/i-InAlAs, and (c) 50 nm-thick p-InAlAs. An I_G compliance of 5 mA was applied for all measurements.

We interpreted this observation as a possible piece of evidence for hydrogen passivation of defects at the wafer-bonded interface as already discussed in the Ga-polar BAVET section above. Based on theoretical investigations performed by first-principles calculations [40], [46], it is deducible that the formation energy of hydrogen is the lowest in a form of H^- (*i.e.* behaving as an acceptor) in n-type InGaAs, which is the constituting material for the BAVET channel situated immediately adjacent to the WBI.

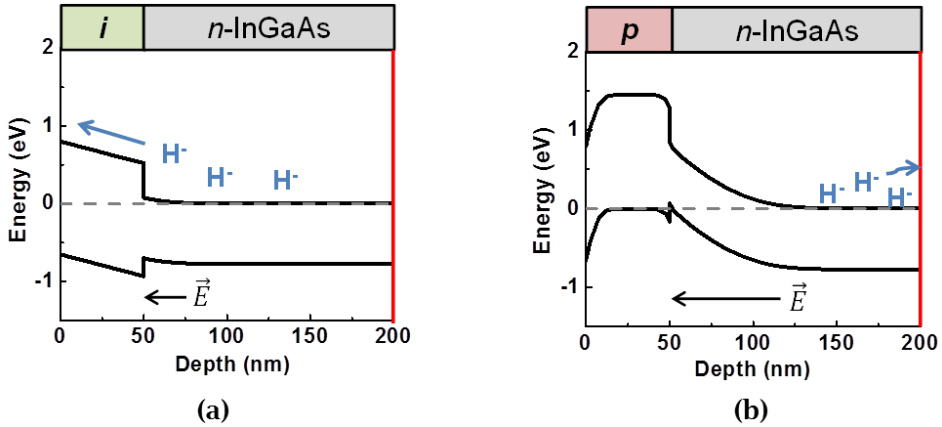


FIGURE 34. Energy band diagrams of III-As structures with an (a) i-InAlAs and (b) p-InAlAs gate barrier and illustrated behavior of H^- in the n-InGaAs channel.

Fig. 34(a)-(b) illustrate the two contrasting behaviors of the H^- present in the *n*-InGaAs channel with either the *i*-InAlAs or *p*-InAlAs gate heterobarrier, which have been

predicted based on the different internal electric fields as well as the heights of the effective gate barrier potentials. As shown in Fig. 34(a), it would be easier for the H^- to escape the structure with the *i*-InAlAs gate heterobarrier due to the narrower depletion region in the channel and lower effective barrier. Conversely, in the case of the *p*-InAlAs structure depicted in Fig. 34(b), the energy bands are set up in the manner that the H^- cannot as easily escape, thus making them linger near the WBI and passivate the defects. As a side note, if the hydrogen passivation truly happens near the WBI, the WBI defects could be donor-like, *i.e.* positively charged.

23.4. N-polar InGaN Thickness Series Study

Another important design knob available in the BAVET structure is the thickness of InGaN layer on top of the GaN drain material, which effectively serves as an interlayer between III-As channel and GaN drain. The $In_{0.05}Ga_{0.95}N$ thickness has been varied as: 0 nm, 5 nm, 10 nm, 15 nm, and 25 nm in the BAVETs with the i-InAlAs as their gate heterobarrier, and the measured *I-V* characteristics are as shown in Fig. 35(a)-(e).

It is immediately observed that the BAVET with 0 nm-thick InGaN interlayer (GaN only) exhibits an extremely low current, only flowing ~135 mA/mm at a very high applied V_{DS} of 12 V and thus showing a very poor device conductance. A noticeable improvement is made in the BAVET with a 5 nm-thick InGaN interlayer shown in Fig. 35(b) in comparison to the BAVET with no InGaN interlayer, but the overall device resistance is fairly high, showing a clear degradation in the transconductance as well as an extremely low R_{ON}. A BAVET with a 10 nm-thick InGaN interlayer is shown in Fig. 35(c), exhibiting a substantially reduced turn-on voltage and a high drain current of 600 mA/mm at V_{GS} = 0 V and V_{DS} = 8 V. As the InGaN interlayer thickness increased to values greater than 10 nm, it is observed that the turn-on voltage increases while the maximum current decreases.

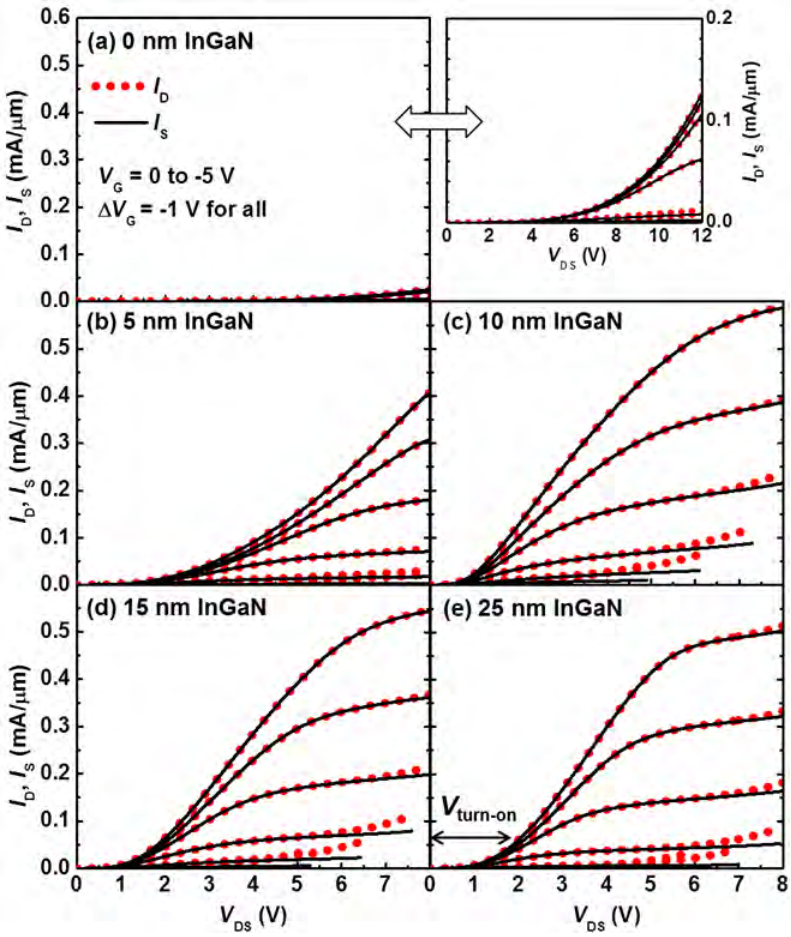


FIGURE 35. Measured output characteristics of N-polar BAVETs with a (a) 0 nm-, (b) 5 nm-, (c) 10 nm-, (d) 15 nm-, and (e) 25 nm-thick N-polar *n*-InGaN interlayer. All BAVETs have dimensions of L_{ap} = 6 μm, L_{go} = 2 μm, and W = 75 × 2 μm.

In the N-polar BAVET with a 10 nm-thick InGaN interlayer, it is predicted that a 2DEG is fully induced at the InGaN/GaN interface, which in turn would pull the energy bands of the InGaN interlayer steeply downwards as depicted in Fig. 36. In this scenario, the barrier at the InGaN/GaN interface would be effectively eliminated due to presence of the 2DEG, and the effective barrier at the InGaAs/InGaN WBI would become much more transparent to the electrons that tunnel into the III-N from the InGaAs channel. In this light, it is also reasonable to postulate that the primary transport mechanism for electrons through the WBI is the thermionic-field emission.

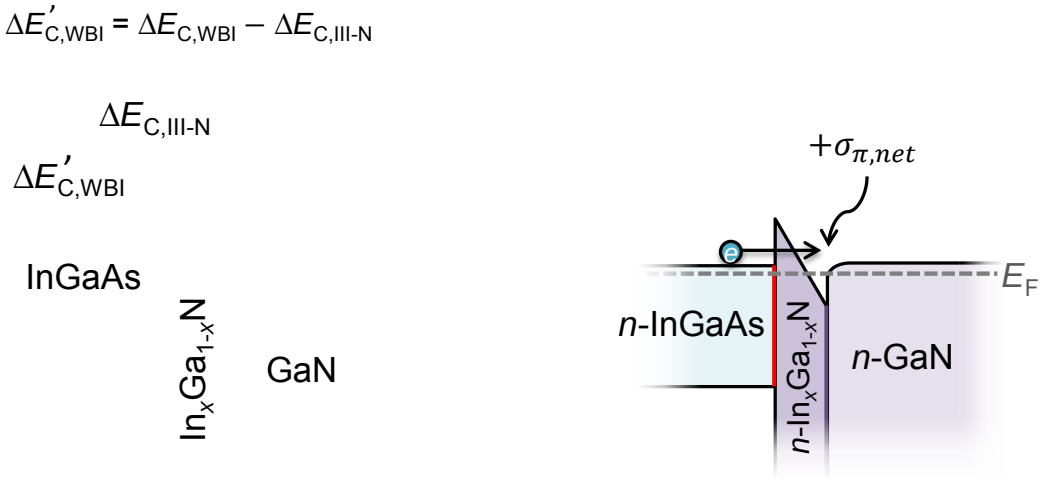


FIGURE 36. Energy band diagram of *n*-InGaAs/N-polar *n*-InGaN/*n*-GaN drawn with the electric field. The presence of the net positive polarization induced charge induces a 2DEG at the N-polar InGaN/GaN interface, thus introducing a steep band bending of the InGaN interlayer.

23.5. Eliminating the BAVET Turn-On Voltage

We have taken the previously examined gate electrode geometry study discussed in Ga-polar BAVET section and applied it to the N-polar BAVET study as well. The two gate geometries utilized in this section are depicted in Fig 37(a)-(b). Fig. 37(a) depicts a "solid-gate" geometry, where the entire aperture region is covered with the gate metal, whereas Fig. 37(b) depicts the "split-gate" geometry, where only the regions that overlap the CBL below are covered with the gate metal.

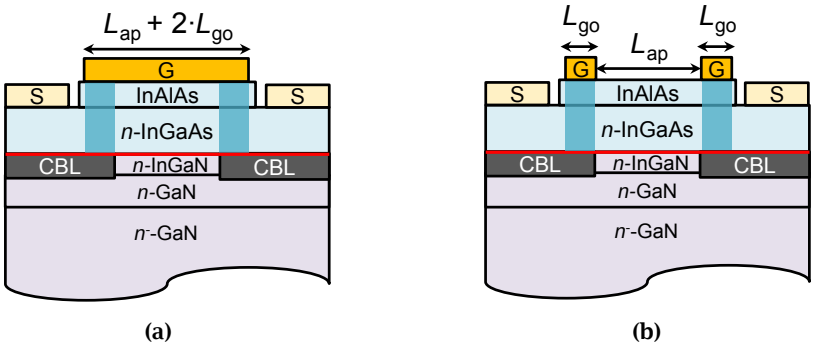


FIGURE 37. Cross-sectional schematics of BAVETs with two different gate electrode geometries of (a) "solid-gate" and (b) "split-gate." The shaded region with darker blue is where the modulation of current actually occurs.

As shown in Fig. 38(c), the *I-V* of the p-InAlAs BAVET with the split-gate exhibits a smaller turn-on voltage, lower $V_{DS,sat}$, and lower gate leakage when compared to the p-InAlAs BAVET with the solid-gate depicted in Fig. 38(b). Due to the absence of any gate-connected field plate likely enabling the re-distribution of the electric field over a larger region, the peak electric field at the edges of the split-gate electrodes is expected to be higher than in the case of the solid-gate. Hence, the improved behavior of the p-InAlAs BAVETs with the use of the split-gate geometry implies that the higher peak electric field triggers beneficial effects which are not yet understood.

The impact ionization, which is believed to occur in the i-InAlAs BAVET with the split-gate at high electric field (as mentioned in the Ga-polar BAVET discussion) is not observed in the p-InAlAs BAVET with the split-gate. This contrasting observation seen in the p-InAlAs BAVETs can due to the lower net electric field in the system due to its less negative threshold voltage than the i-InAlAs BAVETs.

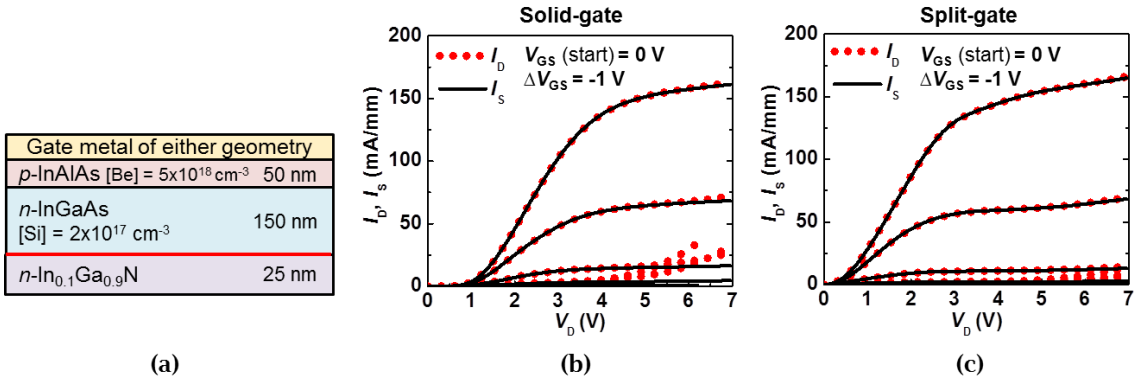


FIGURE 38. (a) Details of the key layers present in these BAVETs. Measured *I-V* characteristics of (b) solid-gate and (c) split-gate BAVETs with L_{ap} = 6 μm, L_{go} = 2 μm, and W = 75 × 2 μm.

In an attempt to further improve the BAVET performance, an idea of implementing a p-InGaAs/i-InAlAs bilayer as the gate heterobarrier was also explored. The use of the p-InGaAs based gate heterobarrier on InP-based FETs was previously explored by Hashemi *et al*. [47], [48]. From these studies, it was found that the introduction of a valence band discontinuity (ΔE_V) due to the presence of the p-InGaAs can effectively mitigate the hole injection into the channel when the gate is under forward bias. This allows for a larger voltage swing, while delaying the occurrences of any degradation in the *I-V*

characteristics that are associated typically with the more positive voltages applied on the gate. The simulated energy band diagram of the III-As region with a 35/15 nm p-InGaAs/i-InAlAs bilayer gate heterobarrier is shown in Fig. 39.

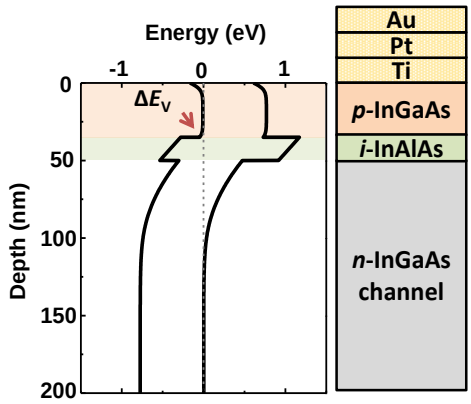


FIGURE 39. Simulated energy band diagram of a 35/15/150 nm *p*-InGaAs/*i*-InAlAs/*n*-InGaAs structure with an arrow indicating the valence band discontinuity.

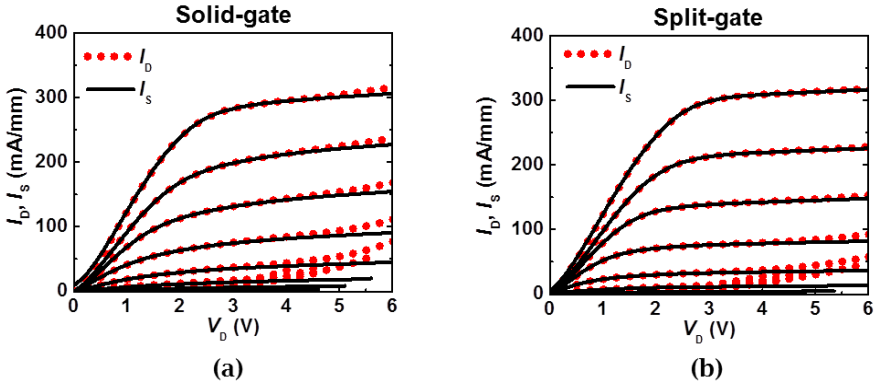


FIGURE 40. *I-V* characteristics measured with V_{GS} (start) = 1 V of the *p*-InGaAs/*i*-InAlAs BAVETs with the (a) solid-gate and (b) split-gate geometries. Both BAVETs have L_{ap} = 4 μm, L_{go} = 2 μm, and W = 75 × 2 μm.

The measured *I-V* characteristics of BAVETs, which contain the p-InGaAs/i-InAlAs gate heterobarrier with (a) solid-gate and (b) split-gate geometry, are shown in Fig. 40(a)-(b). They both have 10 nm-thick InGaN interlayer, which was proven to be the most optimized thickness for the N-polar BAVETs under investigation. It is clearly observed that the overall device performance has further improved by implementing the p-InGaAs

in the gate heterobarrier. Furthermore, it is observed that the combination of the p-InGaAs/i-InAlAs gate heterobarrier with the split-gate electrode geometry further improves the turn-on voltage and the leakage current. We have successfully achieved fully functional wafer-bonded transistors using completely dissimilar channel/collector material using the direct wafer-bonding technology, thus showing promise in future wafer-bonding applications for other electronic devices.

Conclusion

Wafer-bonding is a novel technique which enables realizations of heterostructures consisting of heteroepitaxy-incompatible materials with a large lattice mismatch. Since its discovery, wafer-bonding has continued to expand its impact in diverse applications related to the field of semiconductors—from silicon-on-insulator wafers to hybrid III-V/Si photonics to many more. Likewise, if high-quality wafer-bonded heterostructures with unique combinations of materials can be successfully demonstrated, it is evident that their implementation in electronic devices will result in several breakthroughs.

Acknowledging the potential of wafer-bonding in expanding the design space in the field of electronics, a concept of a wafer-bonded transistor consisting of a III-As channel (with superior carrier transport properties) and III-N drain (with very high breakdown voltage) has been developed with the aim of simultaneously achieving both the high-frequency and high-power performances within a single device. The transistor design selected for the wafer-bonded heterojunctions of III-As/III-N is the current aperture vertical electron transistor (CAVET), from which the regrown AlGaN/GaN channel with a two-dimensional electron gas is substituted with a wafer-bonded InGaAs channel.

By performing elaborated series studies on the doping in the gate heterobarrier, thickness of the added InGaN interlayer and gate electrode geometry, the inherent problems seen in the BAVETs could be better understood and partly addressed. Finally, in the latest generation BAVET designed with all of the key observations taken into account, the turn-on voltage, which has been a persistent problem observed from the majority of the functional wafer-bonded transistors studied so far, was nearly completely eliminated, thus showing promise in expanding the use of wafer-bonding into the field of electronic devices.

Bibliography

[1] Kish, F. A.; Vanderwater, D. A.; DeFevere, D. C.; Steigerwald, D. A.; Hofler, G. E.; Park, K. G.; Steranka, F. M.; "Highly reliable and efficient semiconductor wafer-bonded AlGaInP/GaP light-emitting diodes," *Electronics Letters*, vol.32, no.2, pp.132 (1996).

[2] Tanabe, K.; Morral, A.; Atwater, H. A.; Aiken, D. J.; Wanlass, Mark W.; "Direct-bonded GaAs/InGaAs tandem solar cell," *Applied Physics Letters*, vol.89, no.10, pp.102106 (2006).

[3] Toledo, N.; "Design of Integrated III-Nitride/Non-III-Nitride Multijunction Photovoltaic Devices", *PhD Thesis* (2012).

[4] M. Urteaga, R. Pierson, P. Rowell, V. Jain, and M. Rodwell, *Device Research Conference* (2011), p. 281.

[5] Kolluri, S.; Keller, Stacia; DenBaars, Steven P.; Mishra, Umesh K., "N-Polar GaN MIS-HEMTs With a 12.1-W/mm Continuous-Wave Output Power Density at 4 GHz on Sapphire Substrate," *Electron Device Letters*, *IEEE* , vol.32, no.5, pp.635,637, May 2011

[6] Snow, E. L.; "InGaAs and GaN FETs via Direct Wafer Bonding", PhD Thesis (2010).

[7] Asif Khan, M. and Bhattarai, A. and Kuznia, J. N. and Olson, D. T., "High electron mobility transistor based on a GaN- AlxGa1−xN heterojunction", *Applied Physics Letters*, 63, 1214-1215 (1993)

[8] J. Albrecht et al., CSICS, IEEE (2010).

[9] Chowdhury, S; Swenson, B. L.; Wong M. H.; Mishra, U. K.; "Current status and scope of gallium nitride-based vertical transistors for high-power electronics application", *Semicond. Sci. Technol.*, 28, p. 074014 (2013)

[10] J. A. del Alamo, "Nanometer-scale Electronics with III–V Compound Semiconductors", *Nature*, vol. 479, pp. 317-323, Nov. 2011.

[11] Gösele, U.; Tong, Q.-Y.; "Semiconductor wafer bonding," *Annual Rev. Mater. Sci.*, vol. 28, no. 1, pp. 215–241, 1998.

[12] Ben-Yaacov, I.; Seck, Y.-K.; Mishra, U. K.; DenBaars, S. P.; "AlGaN/GaN Current Aperture Vertical Electron Transistors with Regrown Channels", *J. Appl. Phys.*, vol. 95, no. 4, pp. 2073-2078, Feb. 2004.

[13] Gao, Y.; Ben-Yaacov, I.; Mishra, U.K.; Hu, E.L., "Optimization of AlGaN/GaN current aperture vertical electron transistor (CAVET) fabricated by photoelectrochemical wet etching," *Journal of Applied Physics*, vol.96, no.11, pp.6925,6927 (2004).

[14] S. Chowdhury, M. H. Wong, B. L. Swenson, and U. K. Mishra, "CAVET on bulk GaN substrates achieved with MBE-regrown AlGaN/GaN layers to suppress dispersion", *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 41-43 (2012).

[15] S. Chowdhury, B.L. Swenson, M.H. Wong, U.K. Mishra, *Semicond. Sci. Technol.*, 28, p. 074014 (2013).

[16] U. K. Mishra and J. Singh, *Semiconductor Device Physics and Design*, Springer-Verlag.

[17] Lal, S.; Jing Lu; Gupta, G.; Thibeault, B.J.; DenBaars, S.P.; Mishra, U.K., "Impact of Gate-Aperture Overlap on the Channel-Pinch Off in InGaAs/InGaN-Based Bonded Aperture Vertical Electron Transistor", *Electron Device Letters, IEEE*, vol.34, no.12, pp.1500,1502, (2013).

[18] M. Grundmann, http://my.ece.ucsb.edu/mgrundmann/bandeng.htm.

[19] S.J. Pearton, "Ion implantation for isolation of III-V semiconductors", *Materials Science Reports*, vol. 4, no. 6, 1990, pp. 313,363 (1990).

[20] J.F. Ziegler, SRIM 2008, http://www.srim.org.

[21] Lal, S.; Lu, J.; Li, H.; Thibeault, B.J.; DenBaars, S.P.; Mishra, U.K., "Saturation Voltage and Virtual Gate in Wafer-Bonded Transistors," in preparation.

[22] Ponce, Fernando A.; "Defects and interfaces in GaN epitaxy", *MRS bulletin*, 22.02, pp.51-57 (1997).

[23] Snow, E. L.; "InGaAs and GaN FETs via Direct Wafer Bonding", *PhD Thesis* (2010).

[24] C. Lian, H. G. Xing, C.-Y Chang, N. Fichtenbaum, "Electrical transport properties of wafer-fused p-GaAs/n-GaN heterojunctions," *Applied Physics Letters*, vol.93, no.11, pp.112103 (2008).

[25] Kim, J; "III-As/N-polar III-N Wafer-Bonded Heterojunctions and Their implementation in Current Aperture Vertical Electron Transistors ", *PhD Thesis* (2015).

[26] Tanabe, K.; Morral, A.; Atwater, H. A.; Aiken, D. J.; Wanlass, Mark W.; "Direct-bonded GaAs/InGaAs tandem solar cell," *Applied Physics Letters*, vol.89, no.10, pp.102106 (2006).

[27] Tanabe, K.; Watanabe, K. ; and Arakawa, Y. ; "III-V/Si hybrid photonic devices by direct fusion bonding," *Sci. Rep.*, 2, 349 (2012).

[28] Kish, F. A.; Vanderwater, D. A.; DeFevere, D. C.; Steigerwald, D. A.; Hofler, G. E.; Park, K. G.; Steranka, F. M.; "Highly reliable and efficient semiconductor wafer-bonded AlGaInP/GaP light-emitting diodes," *Electronics Letters*, vol.32, no.2, pp.132 (1996).

[29] Lian, C.; Xing, H. G.; Wang, C. S.; McCarthy, L.; Brown, D.; "DC Characteristics of AlGaAs/GaAs/GaN HBTs Formed by Direct Wafer Fusion," *Electron Device Letters, IEEE,* vol.28, no.1, pp.8,10 (2007).

[30] Lal, S.; Lu, J.; Gupta, G.; Thibeault, B.J.; DenBaars, S.P.; Mishra, U.K., "Impact of Gate-Aperture Overlap on the Channel-Pinch Off in InGaAs/InGaN-Based Bonded Aperture Vertical Electron Transistor," *Electron Device Letters, IEEE,* vol.34, no.12, pp.1500,1502 (2013).

[31] Nakayama, K; Tanabe, K.; Atwater, H. A.; "Improved electrical properties of wafer-bonded p-GaAs/n-InP interfaces with sulfide passivation," *Journal of Applied Physics*, vol.103, no.9, pp.094503 (2008).

[32] Vanderwater, D.A.; Kish, F.A.; Peansky, M.J.; Rosner, S.J.; "Electrical conduction through compound semiconductor wafer bonded interfaces," *Journal of Crystal Growth*, vol. 174, no. 1–4, pp. 213 (1997).

[33] Kim, J.; Toledo, N. G.; Lal, S.; Lu, J.; Buehl, T. E.; Mishra, U. K.; "Wafer-Bonded p-n Heterojunction of GaAs and Chemomechanically Polished N-Polar GaN," *Electron Device Letters, IEEE*, vol.34, no.1, pp.42 (2013).

[34] Carter, R.J.; Cartier, E.; Kerber, A.; Pantisano, L.; Schram, T.; De Gendt, S.; and Heyns, M.; "Passivation and interface state density of SiO2/HfO2-

based/polycrystalline-Si gate stacks," *Applied Physics Letters*, vol.83, no.3, pp.533 (2003).

[35] Carter, A. D.; Mitchell, W. J.; Thibeault, B. J.; Law, J. J. M.; and Rodwell, M. J. W.; "Al2O3 growth on (100) In0.53Ga0.47As initiated by cyclic trimethylaluminum and hydrogen plasma exposures," *Appl. Phys. Express*, 4 (2011) 091102.

[36] United States Patent Application entitled "Hydrogen passivation of Integrated Circuits," US Appl. No. 20110079884 A1, filed Apr 7, 2011.

[37] Johnson, N. M.; "Hydrogen in compound semiconductors," *Mat. Res. Soc. Symp. Proc.,* vol. 262, pp.369 (1992).

[38] Van de Walle, Chris G.; and Neugebauer, Jörg; "Hydrogen in Semiconductors," *Annual Review of Materials Research*, vol. 36, pp. 179 (2006).

[39] Pavesi, L. and Giannozzi, P.; "Atomic and molecular hydrogen in gallium arsenide: A theoretical study," *Phys. Rev. B*, vol. 46, no. 8, pp. 4621 (1992).

[40] Van de Walle, Chris G.; Neugebauer, J.; "Universal alignment of hydrogen levels in semiconductors, insulators and solutions," *Nature*, vol. 423, no. 6940, pp. 626 (2003).

[41] S. Lal, E. Snow, J. Lu, B. Swenson, S. Keller, S. DenBaars, and U. Mishra, "InGaAs-InGaN Wafer-Bonded Current Aperture Vertical Electron Transistors (BAVETs)", *J. Electronic Materials*, vol. 41, no. 5, pp. 857-864, Feb. 2012.

[42] Lal, S.; Lu, J.; Li, H.; Thibeault, B.J.; DenBaars, S.P.; Mishra, U.K., "Saturation Voltage and Virtual Gate in Wafer-Bonded Transistors," in preparation.

[43] Lal, S.; Lu, J.; Thibeault, B.J.; DenBaars, S.P.; Mishra, U.K., "Drain Resistance at Wafer-Bonded Interface of Unipolar Vertical Transistor and A Method to Mitigate the Same," in preparation.

[44] Lal, S.; Lu, J.; Thibeault, B.J.; DenBaars, S.P.; Mishra, U.K., "Enhancing Critical Field to Impact Ionization in Bonded Current Aperture Vertical Transistors," in preparation.

N-polar References:

[45] S. Keller, C. S. Suh, N. A. Fichtenbaum, M. Furukawa, R. Chu, Z. Chen, K. Vijayraghavan, S. Rajan, S. P. DenBaars, J. S. Speck, and U. K. Mishra, *J. of Appl. Phys.*, vol. 104, 093510, Nov. 2008.

[46] C. G. Van de Walle, J. R. Weber, and A. Janotti, "Role of hydrogen at germanium/dielectric interfaces," *Thin Solid Films*, vol. 517, no. 1, pp. 144–147, Nov. 2008.

[47] M. M. Hashemi, J. B. Shealy, S. P. DenBaars, and U. K. Mishra, "High-Speed p+ GaInAs-n InP Heterojunction JFET's (HJFET's) Grown by MOCVD," *IEEE Electron Device Lett.*, vol. 14, no. 2, pp. 60–62, Feb. 1993.

[48] M. M. Hashemi, J. B. Shealy, P. J. Corvini, S. P. DenBaars, and U. K. Mishra, "High-Performance Inp JFETs Grown by MOCVD Using Tertiarybutylphosphine," *Journal of Electronic Materials*, vol. 23, no. 2, pp. 233–237, Feb. 1994.

List of Publications Funded by this Project

[1] S. Lal, E. Snow, J. Lu, B. Swenson, S. Keller, S. P. Denbaars, and U. K. Mishra, "InGaAs-InGaN wafer-bonded current aperture vertical electron transistors (BAVETs)", *J. Electronic Materials*, vol. 41, no. 5, pp. 857-864, Feb. 2012.

[2] S. Lal, J. Lu, B. Thibeault, S. P. DenBaars, and U. K. Mishra, "Experimental demonstration of a wafer-bonded heterostructure based unipolar transistor with In0.53Ga0.47As channel and III-N drain", *Proc. of Device Research Conference*, pp.165-166, Jun. 2012.

[3] S. Lal, J. Lu, S. Keller, B. Thibeault, S. P. DenBaars, and U. K. Mishra, "Impact of Vertical Leakage on the DC Performance of a Wafer-Bonded Aperture Unipolar Transistor", *Proc. of International Symposium on Compound Semiconductors*, pp. 23, Aug. 2012.

[4] S. Lal, J. Lu, B. Thibeault, S. Keller, S. P. DenBaars, and U. K. Mishra, "Comparative Study of the DC Characteristics and the Impact of Gate-Field-Plate in III-As/InGaN-based and III-As/GaN-based Wafer-Bonded Vertical Aperture Transistors", *Proc. of International Workshop on Nitride Semiconductors,* pp. 335*, Oct. 2012*.

[5] J. Kim, S. Lal, J. Lu, S. P. DenBaars, and U. K. Mishra, "Experimental Demonstration of a Chemo-Mechanically Polished N-polar GaN/III-As Wafer Bonded Current Aperture Vertical Electron Transistor," *Proc. of International Workshop on Nitride Semiconductors*, pp. 300*,* Oct. 2012.

[6] J. Kim, N. G. Toledo, S. Lal, J. Lu, T. E. Buehl, and U. K. Mishra, "Wafer-Bonded p-n Heterojunction of GaAs and Chemomechanically Polished N-Polar GaN," *IEEE Electron Device Lett.*, vol. 34, no. 1, Jan. 2013.

[49] Lal, S.; Lu, J.; Gupta, G.; Thibeault, B.J.; DenBaars, S.P.; Mishra, U.K., "Impact of Gate-Aperture Overlap on the Channel-Pinch Off in InGaAs/InGaN-Based Bonded Aperture Vertical Electron Transistor," *Electron Device Letters, IEEE,* vol.34, no.12, pp.1500,1502 (2013).

[7] S. Lal, J. Lu, M. Guidry, B. Thibeault, S. P. DenBaars, and U. K. Mishra, "Controlling Electronic Properties of Wafer-Bonded Interfaces among Dissimilar Materials: a Path to Developing Novel Wafer-Bonded Devices", submitted to *Device Research Conference*, (2013).

[8] J. Kim, S. Lal, M. A. Laurent, and U. K. Mishra, "Vertical electron transistors with $In_{0.53}Ga_{0.47}As$ channel and N-polar $In_{0.1}Ga_{0.9}N$/GaN drain achieved by direct wafer-bonding," *72*nd *Annu. Device Res. Conf. Digest*, 221, 2014.

[9] J. Kim, M. A. Laurent, H. Li, S. Lal, and U. K. Mishra, "Barrier reduction via implementation of InGaN interlayer in wafer-bonded current aperture vertical electron transistors consisting of InGaAs channel and N-polar GaN drain," *Appl. Phys. Lett.*, 106, 023506, 2015.

[10] S. Lal, J. Lu, B. Thibeault, S. P. DenBaars, and U. K. Mishra, "On the Relationship between the Performance of a Wafer-Bonded Current Aperture Vertical Transistor and Trap Behavior of Wafer-Bonded Interface", *Proc. of International Symposium on Compound Semiconductors*, July 2015.

[11] Lal, S.; Lu, J.; Thibeault, B.J.; DenBaars, S.P.; Mishra, U.K., "Aperture-based Field-Plating to Eliminate Impact Ionization of Channel-Current-blocking region in Wafer-Bonded Vertical Transistors," submitted to Electron Devices, IEEE Trans. on.

1.

1. Report Type

Final Report

Primary Contact E-mail

Contact email if there is a problem with the report.

alex@ece.ucsb.edu

Primary Contact Phone Number

Contact phone number if there is a problem with the report

805-680-7108

Organization / Institution name

University of California, Santa Barbara

Grant/Contract Title

The full title of the funded effort.

N-Face GaN Electronics for Heteroepitaxial and Bonded Structures

Grant/Contract Number

AFOSR assigned control number. It must begin with "FA9550" or "F49620" or "FA2386".

FA9550-10-1-0069

Principal Investigator Name

The full name of the principal investigator on the grant or contract.

Umesh Mishra

Program Manager

The AFOSR Program Manager currently assigned to the award

Kenneth Goretta

Reporting Period Start Date

04/01/2010

Reporting Period End Date

03/31/2015

Abstract

Wafer-bonding is a novel technique which enables realizations of heterostructures consisting of heteroepitaxy-incompatible materials with a large lattice mismatch. Since its discovery, wafer-bonding has continued to expand its impact in diverse applications related to the field of semiconductors—from silicon-on-insulator wafers to hybrid III-V/Si photonics to many more. Likewise, if high-quality wafer-bonded heterostructures with unique combinations of materials can be successfully demonstrated, it is evident that their implementation in electronic devices will result in several breakthroughs.

Acknowledging the potential of wafer-bonding in expanding the design space in the field of electronics, a concept of a wafer-bonded transistor consisting of a III-As channel (with superior carrier transport properties) and III-N drain (with very high breakdown voltage) has been developed with the aim of simultaneously achieving both the high-frequency and high-power performances within a single device. The transistor design selected for the wafer-bonded heterojunctions of III-As/III-N is the current aperture vertical electron transistor (CAVET), from which the regrown AlGaN/GaN channel with a two-dimensional electron gas is substituted with a wafer-bonded InGaAs channel.

By performing elaborated series studies on the doping in the gate heterobarrier, thickness of the added InGaN interlayer and gate electrode geometry, the inherent problems seen in the BAVETs could be better understood and partly addressed. Finally, in the latest generation BAVET designed with all of the key

observations taken into account, the turn-on voltage, which has been a persistent problem observed from the majority of the functional wafer-bonded transistors studied so far, was nearly completely eliminated, thus showing promise in expanding the use of wafer-bonding into the field of electronic devices.

Distribution Statement

This is block 12 on the SF298 form.

Distribution A - Approved for Public Release

Explanation for Distribution Statement

If this is not approved for public release, please provide a short explanation. E.g., contains proprietary information.

SF298 Form

Please attach your SF298 form. A blank SF298 can be found here. Please do not password protect or secure the PDF
The maximum file size for an SF298 is 50MB.

SF298 Mishra.pdf

Upload the Report Document. File must be a PDF. Please do not password protect or secure the PDF . The maximum file size for the Report Document is 50MB.

final report FA9550-10-1-0069.pdf
final report FA9550-10-1-0069.pdf

Upload a Report Document, if any. The maximum file size for the Report Document is 50MB.

Archival Publications (published) during reporting period:

Changes in research objectives (if any):

Change in AFOSR Program Manager, if any:

Extensions granted or milestones slipped, if any:

AFOSR LRIR Number

LRIR Title

Reporting Period

Laboratory Task Manager

Program Officer

Research Objectives

Technical Summary

Funding Summary by Cost Category (by FY, $K)

	Starting FY	FY+1	FY+2
Salary			
Equipment/Facilities			
Supplies			
Total			

Report Document

Report Document - Text Analysis

Report Document - Text Analysis

Appendix Documents

2. Thank You

E-mail user

Aug 19, 2015 15:51:13 Success: Email Sent to: alex@ece.ucsb.edu